

MODEL NAME : *BBV00/BBV10*
PCB NO : *LA-D993P*

BOM P/N :

Dell/Compal Confidential

Schematic Document

KABYLAKE-H

2016-11-01

Rev: 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

EMC@ : Pop of EMI parts

S4G@ : Samsung GDDR5 4G for GPU

M4G@ : Micron GDDR5 4G for GPU

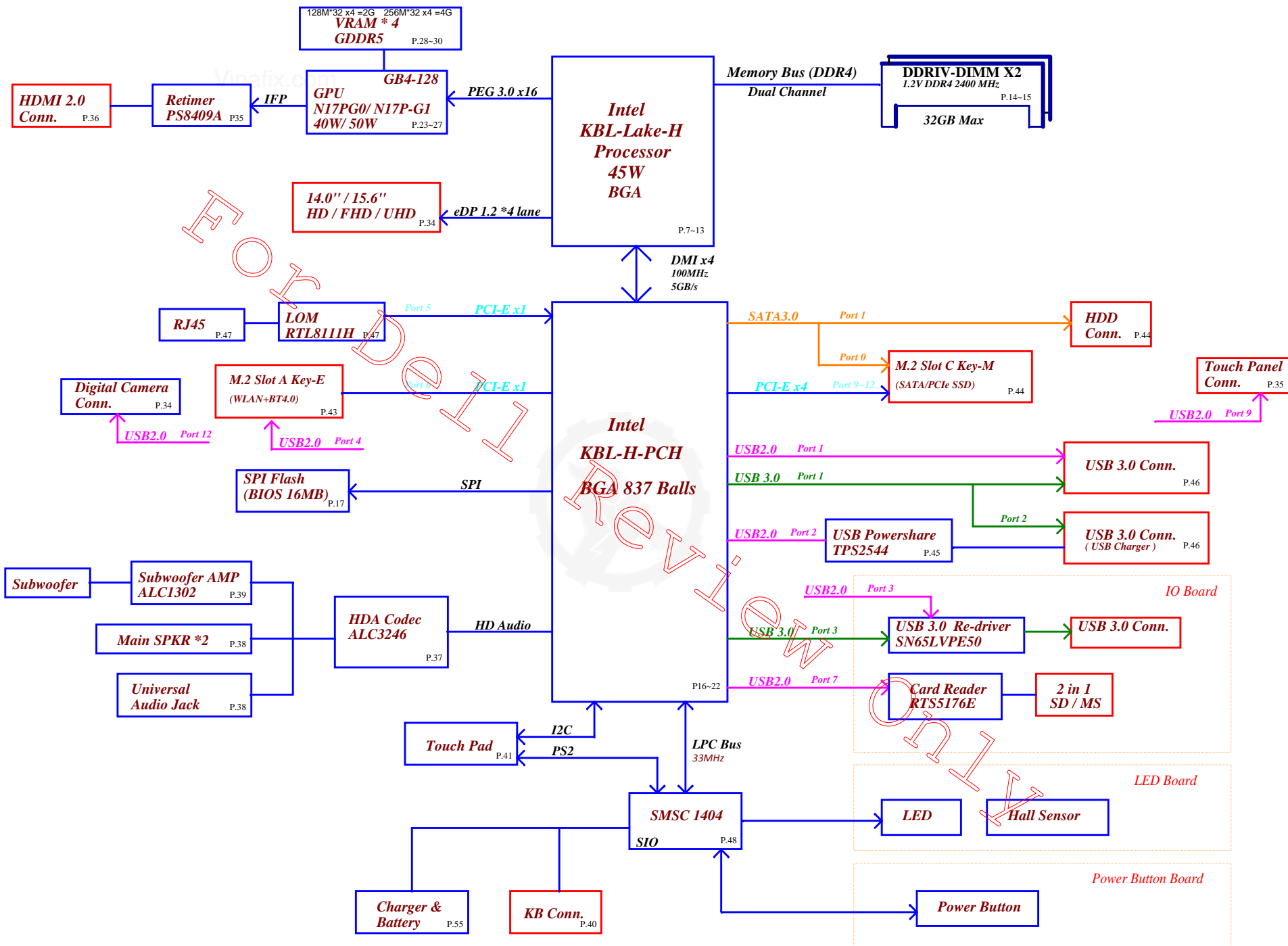
H4G@ : Hynix GDDR5 4G for GPU

BreakDown@ : For measure power consumption

14G0@ : 14" N17P-G0

15G1@ : 15" N17P-G1

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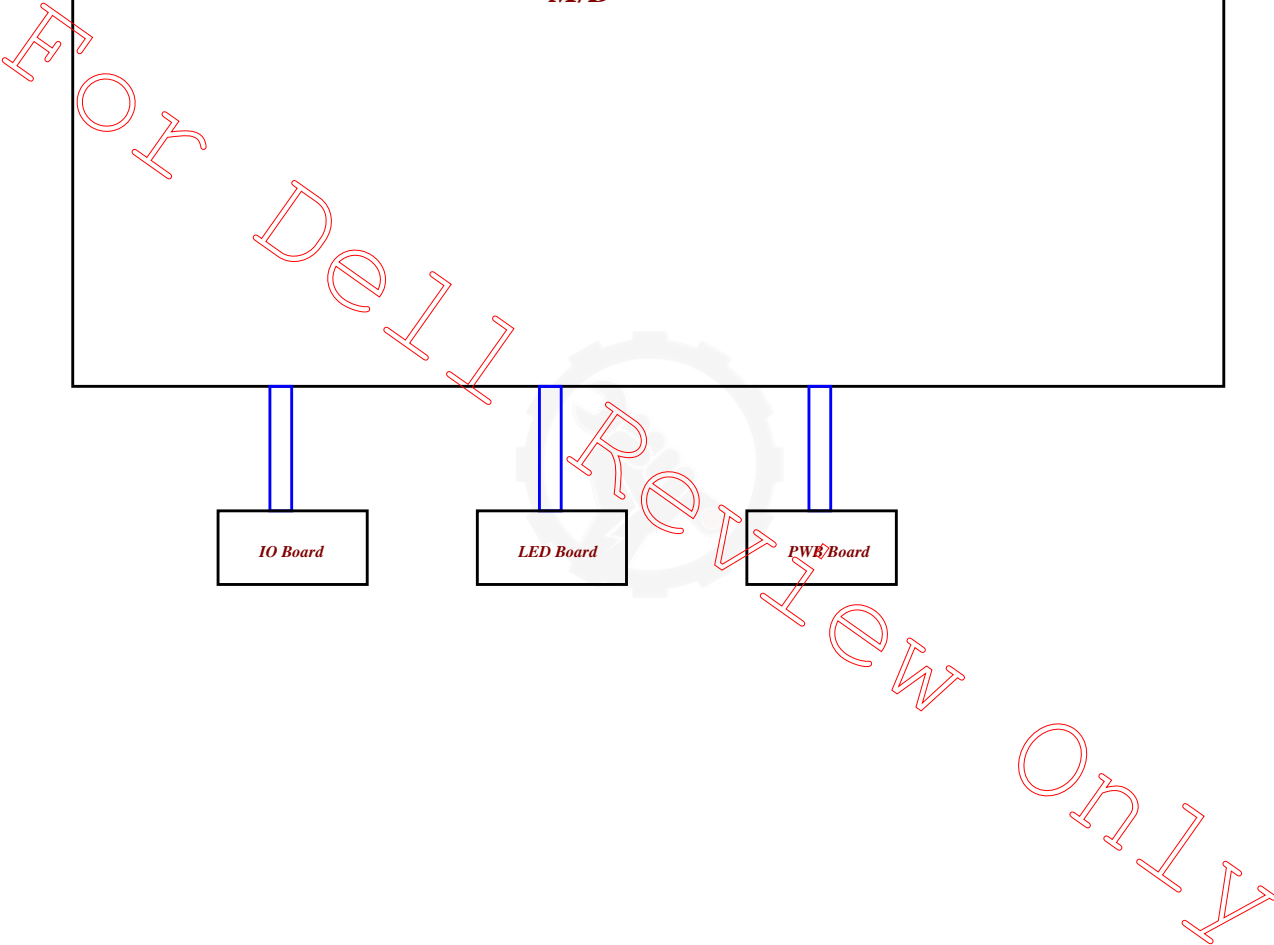


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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
X04	22.1K
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	SSD	0A	SSD
Lane 10	SSD	1A	N/A
Lane 11	SSD	N/A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	Alpine Ridge	2	None
Lane 16		3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

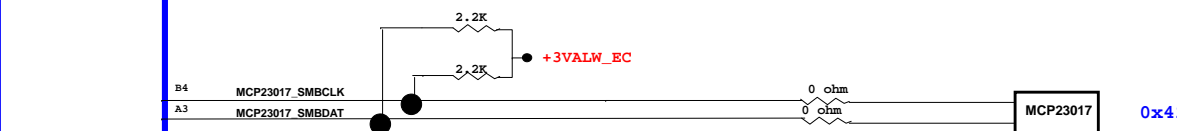
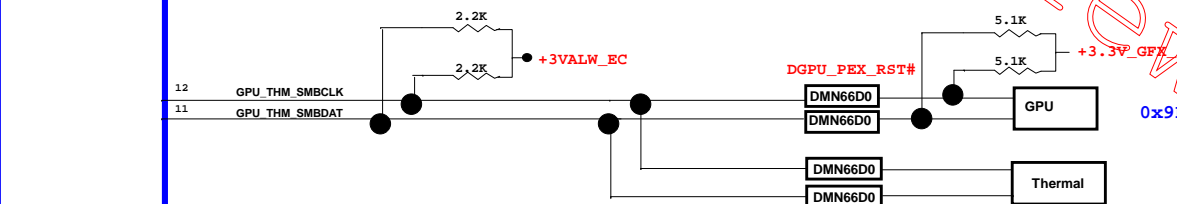
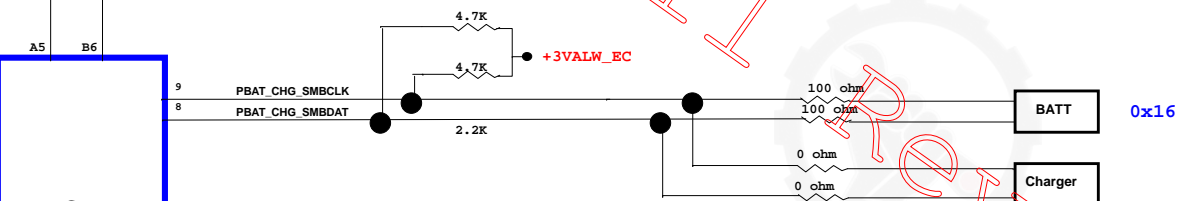
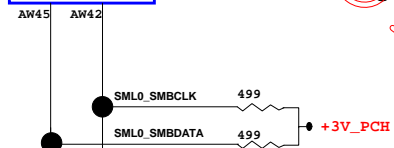
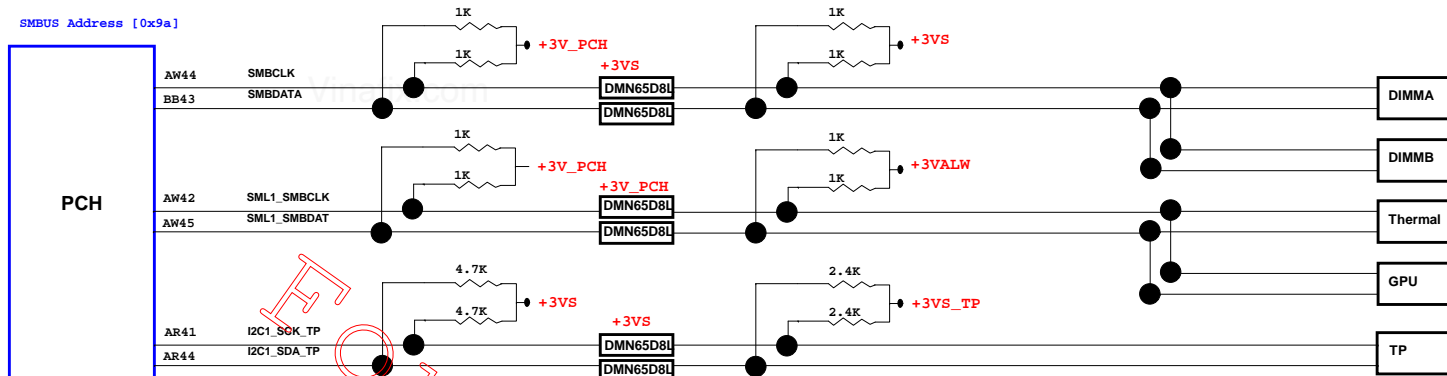
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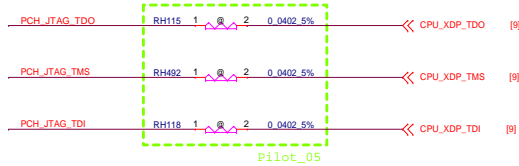
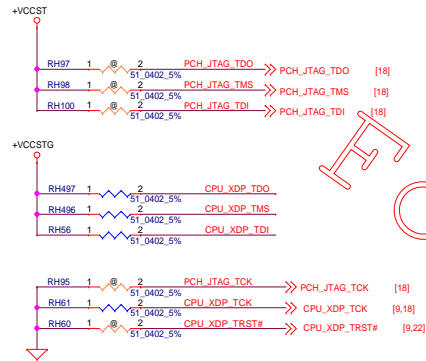
: means Digital Ground



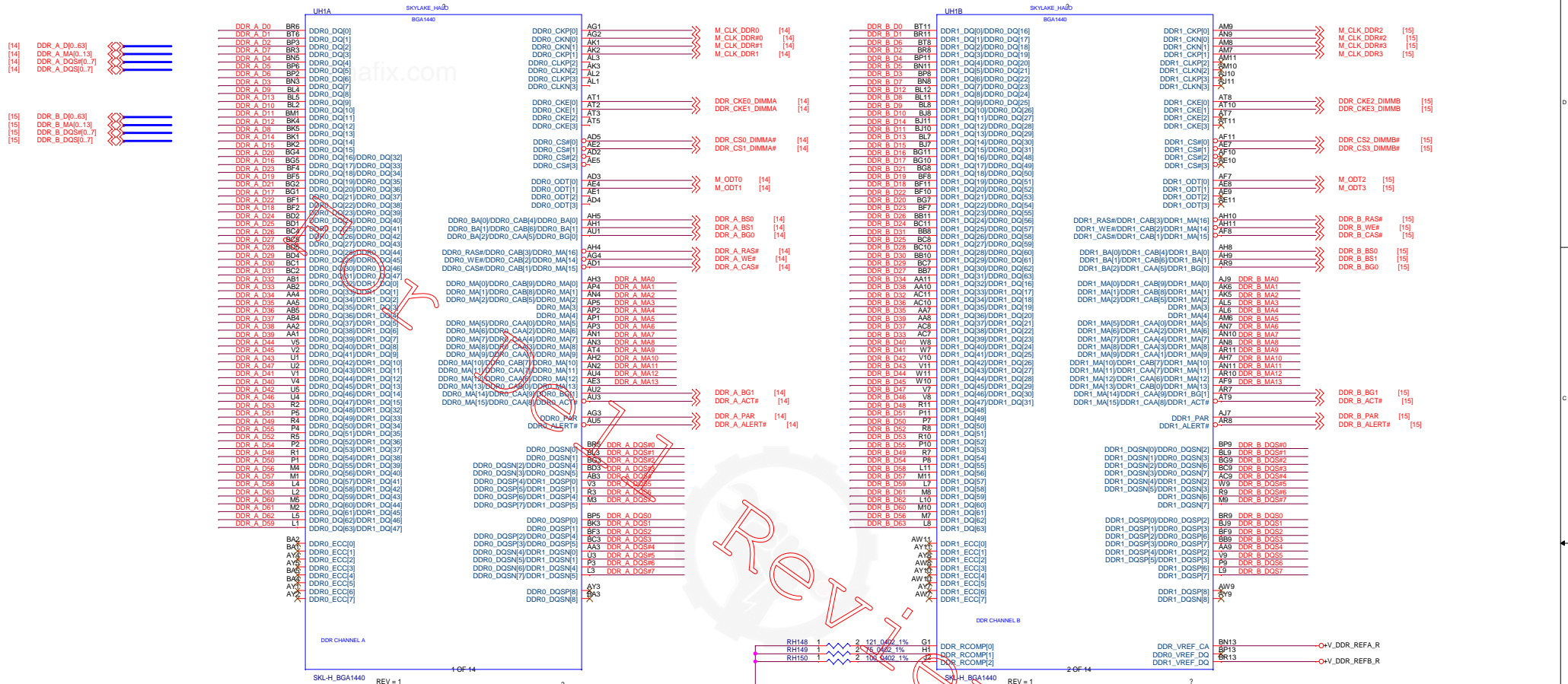
: means Analog Ground



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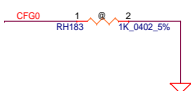


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CFG Straps for Processor

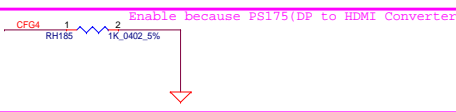
Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



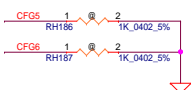
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



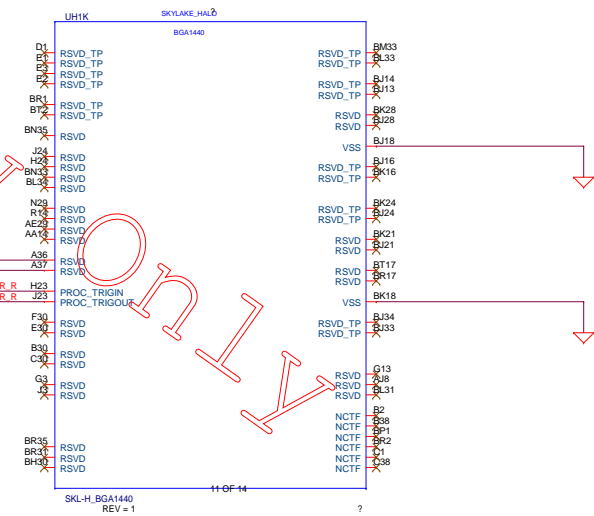
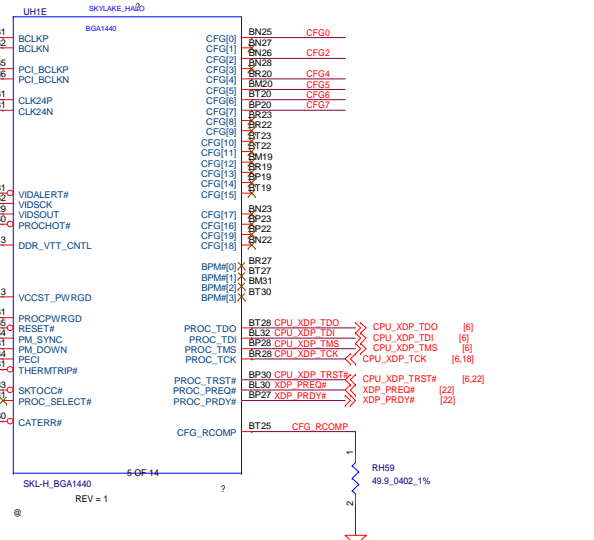
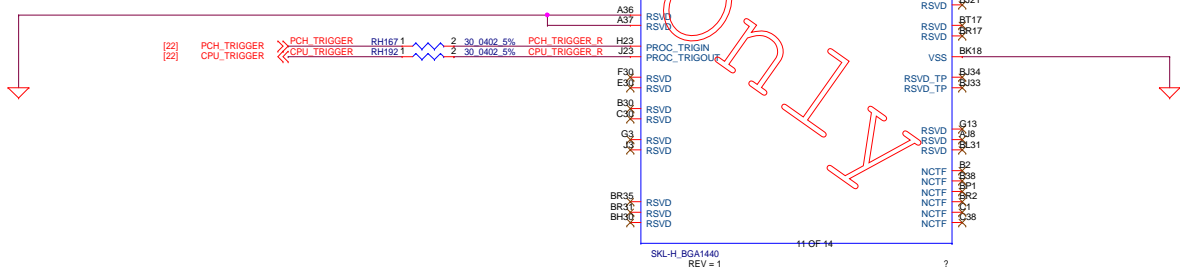
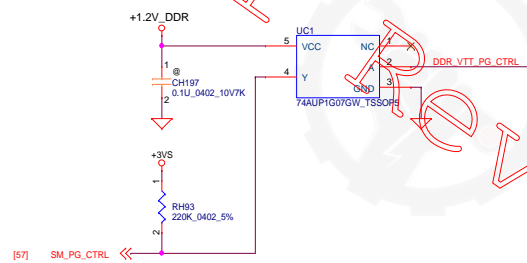
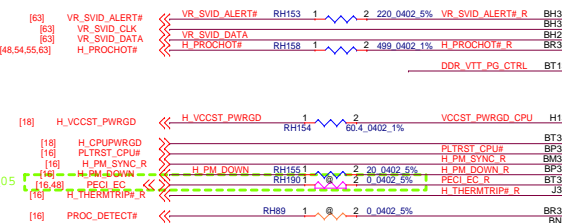
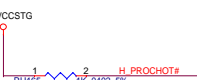
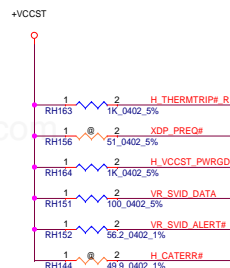
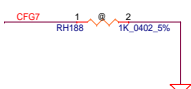
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

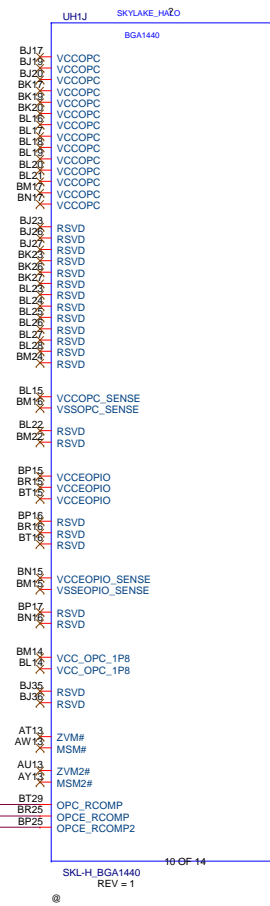
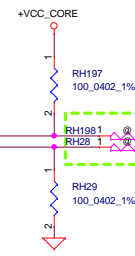
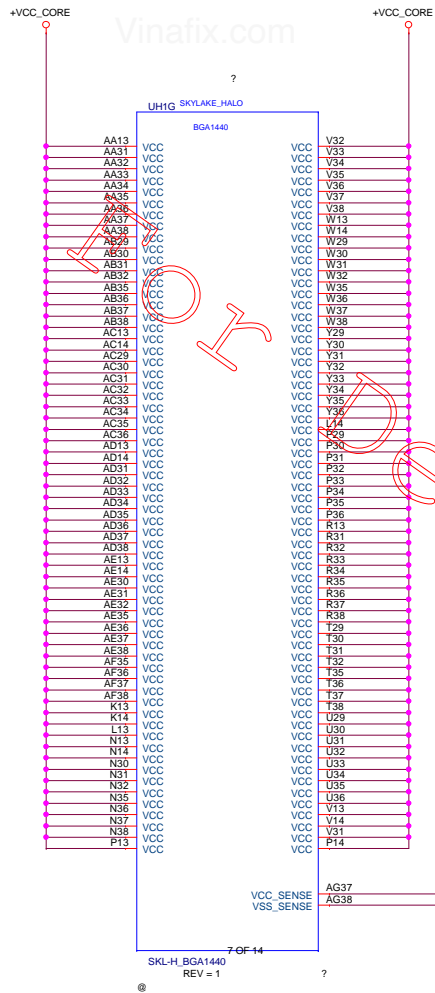


PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



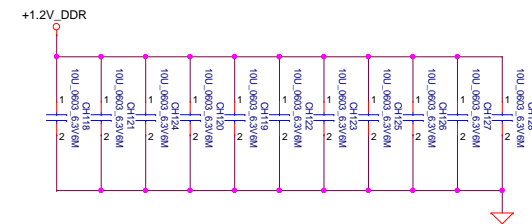
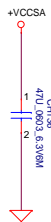
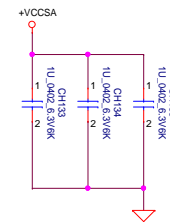
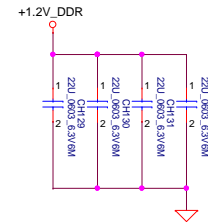
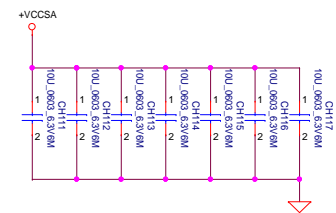
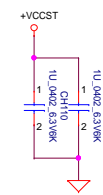
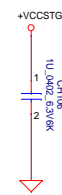
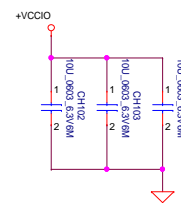
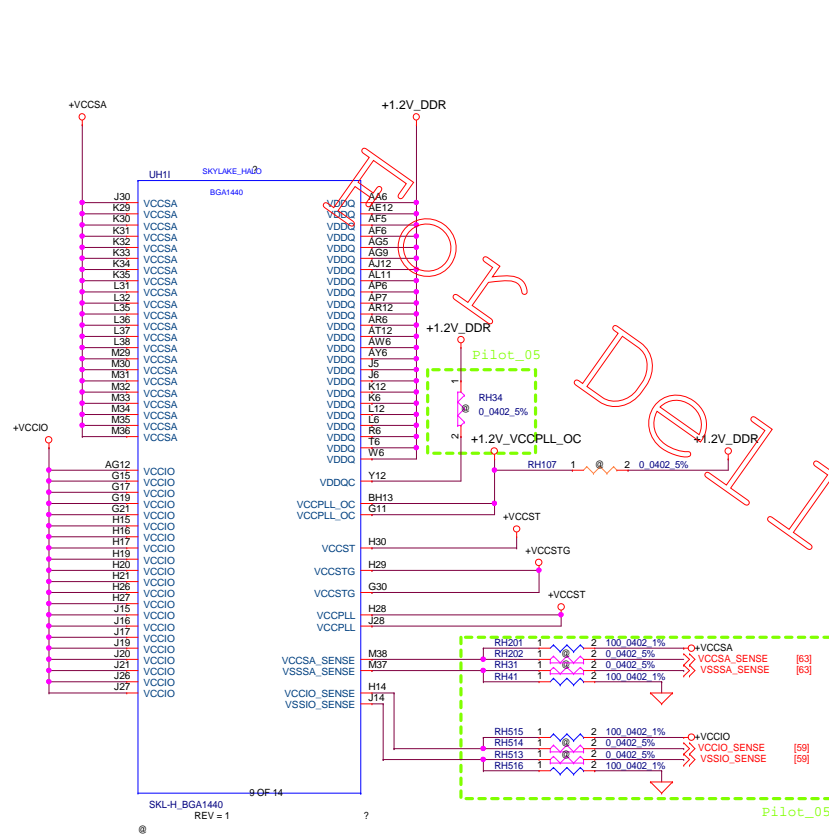
PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



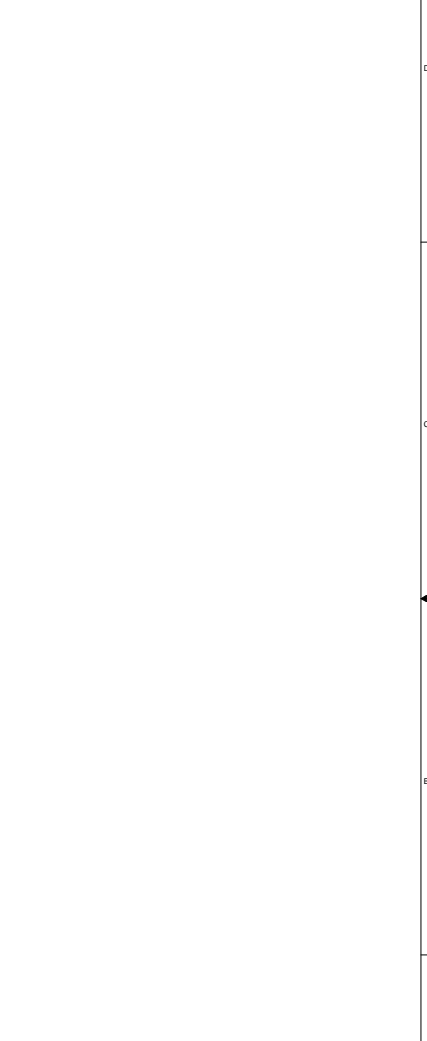
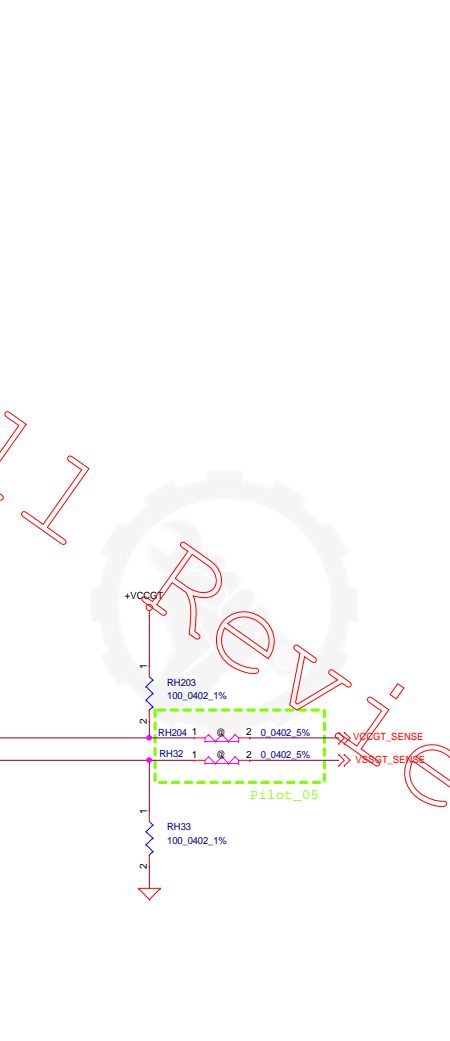
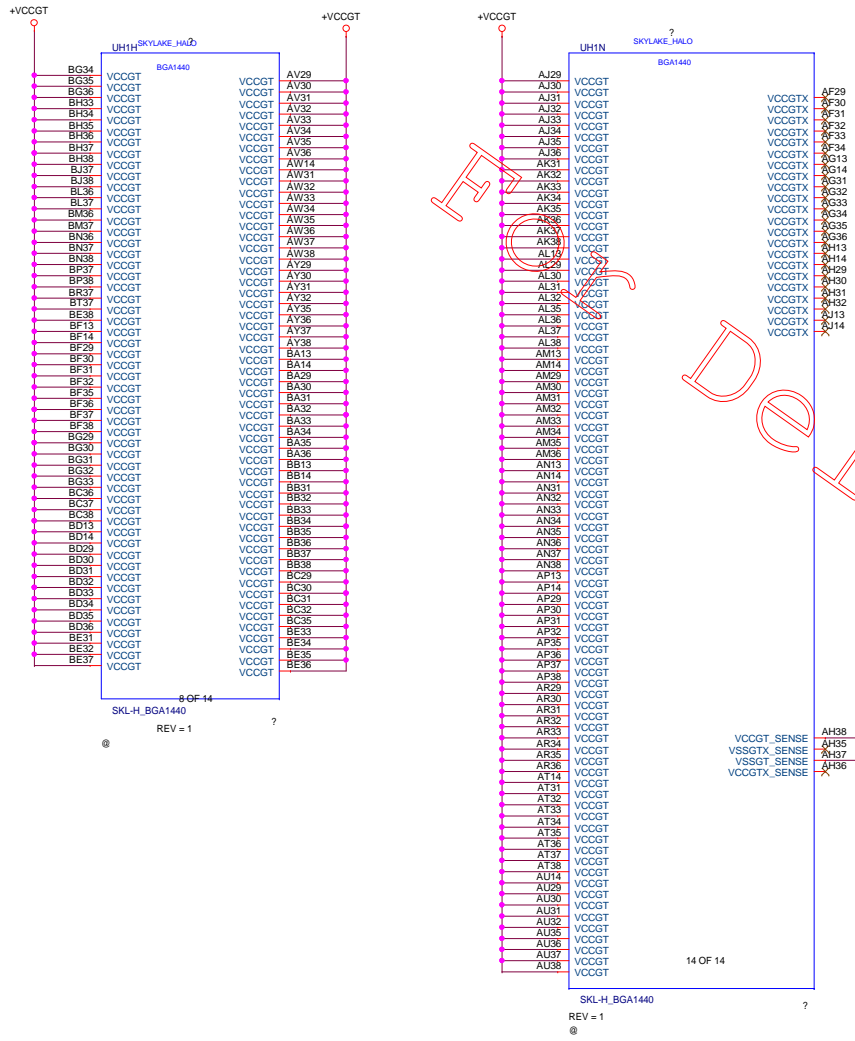


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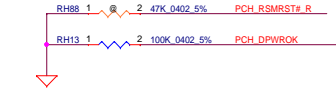
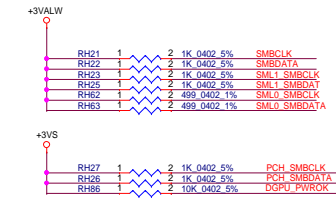
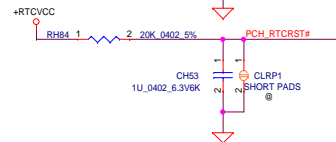
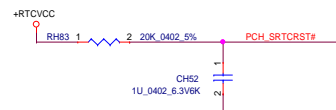
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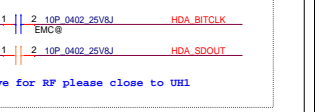
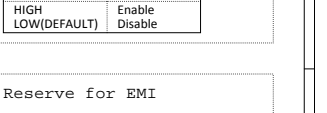
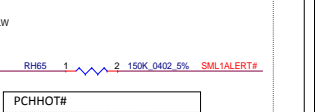
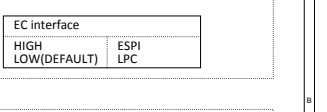
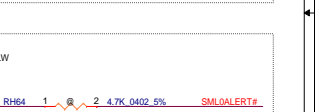
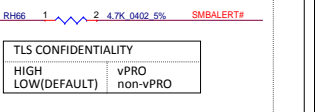
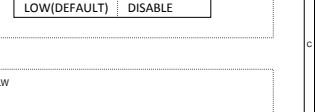
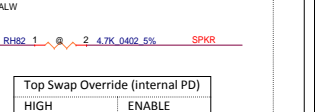
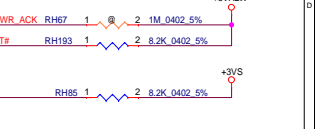
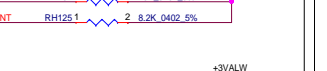
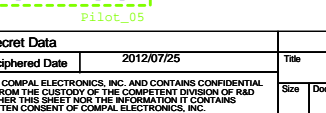
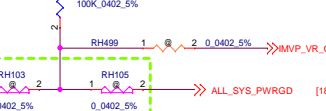
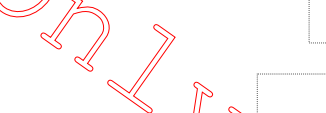
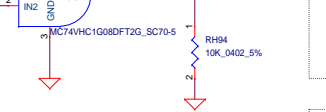
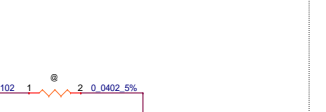
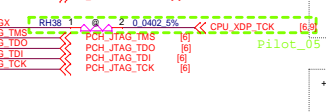
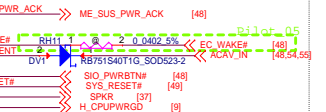
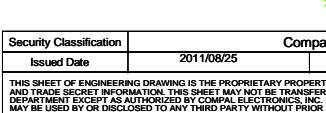
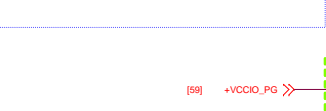
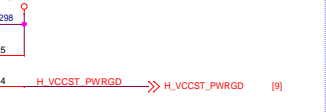
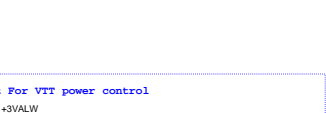
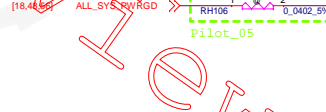
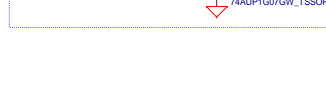
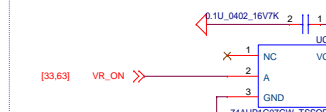
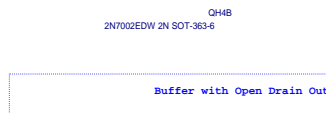
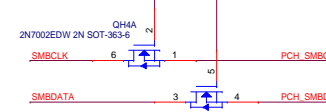
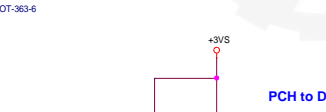
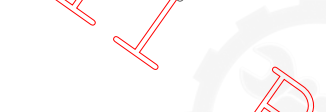
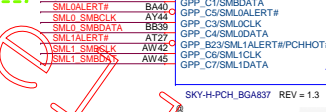
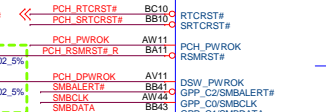
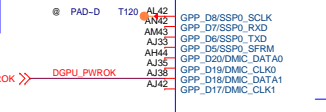
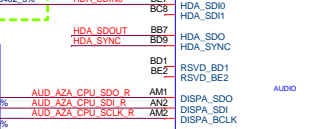
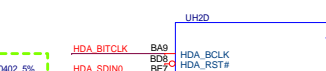
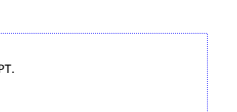
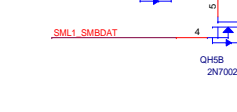
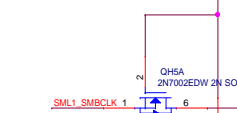
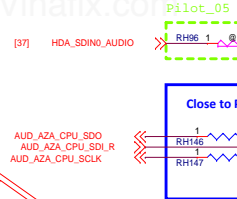
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Date	Tuesday, November 08, 2016	Sheet	12	of 70



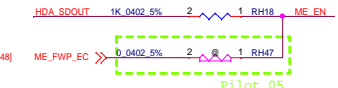
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Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using PPT.

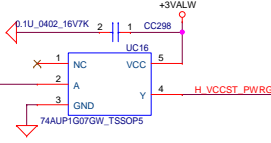


ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) --> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated) --> Pin3 & Pin2 short(Default position)

Buffer with Open Drain Output For VTT power control



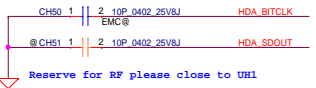
Top Swap Override (Internal PD)
HIGH LOW(DEFAULT) ENABLE DISABLE

TLS CONFIDENTIALITY
HIGH LOW(DEFAULT) vPRO non-vPRO

EC interface
HIGH LOW(DEFAULT) ESPI LPC

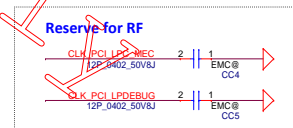
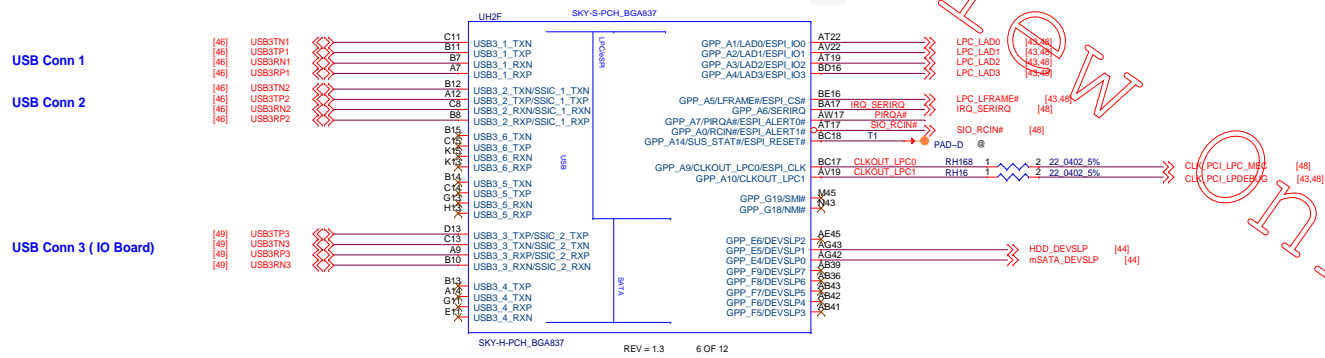
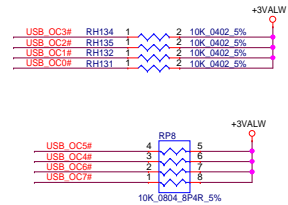
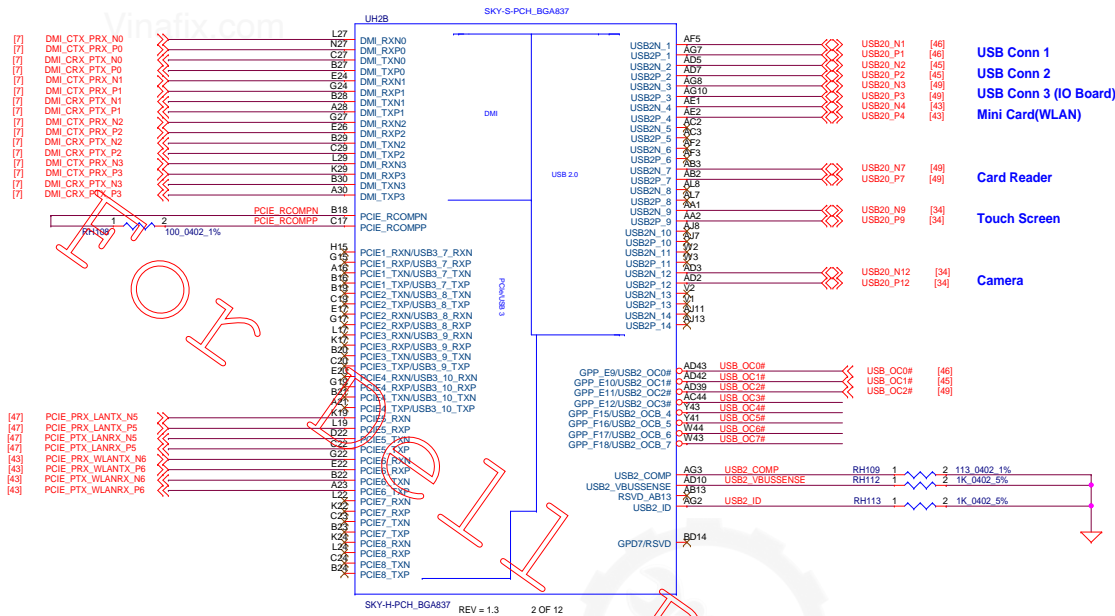
PCHHOT#
HIGH LOW(DEFAULT) Enable Disable

Reserve for EMI

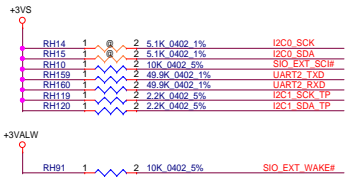


Reserve for RF please close to UH1

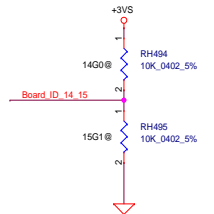
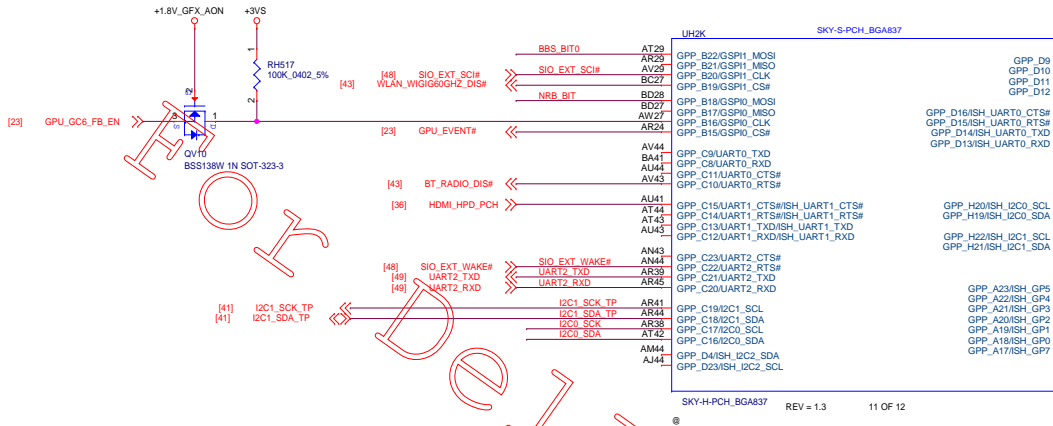
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Issued Date	2011/08/25	Deciphered Date	2012/07/25
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PCH (3/8) DMI,FDI,PM,GFX,DP		Rev	0.1/200
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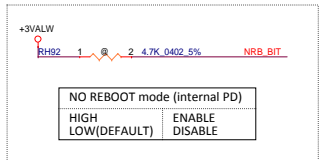
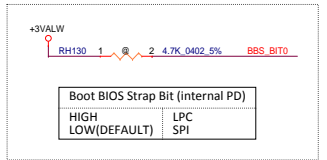
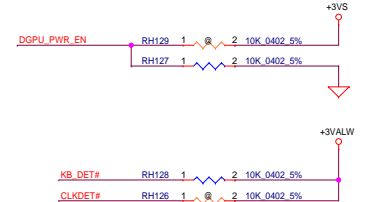
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Issued Date		Deciphered Date		PCH (4/8) PCI, USB	
2011/08/25		2012/07/25		LA-D991P	
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Tuesday, November 08, 2016		19		0.1/000	

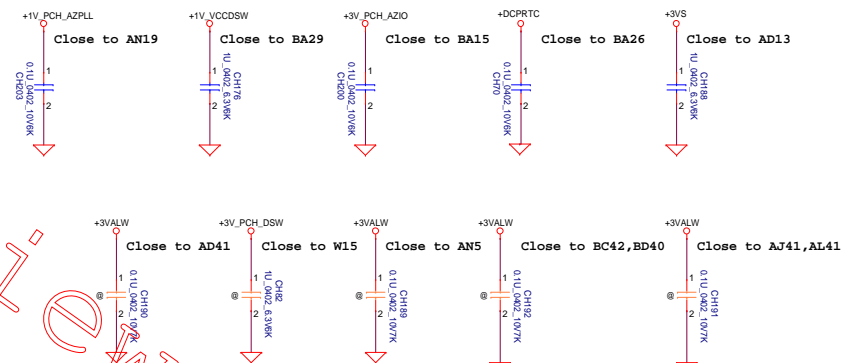
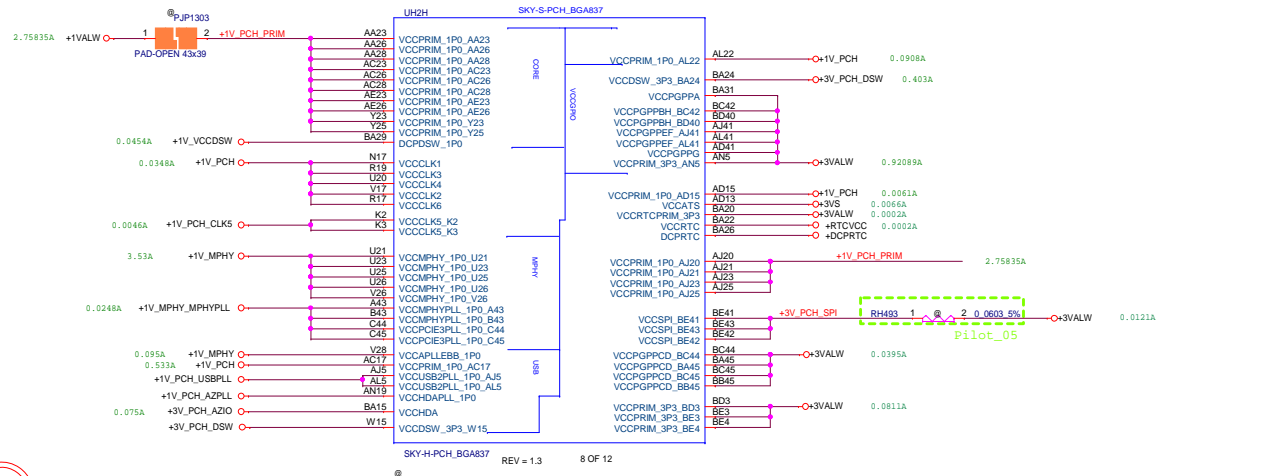
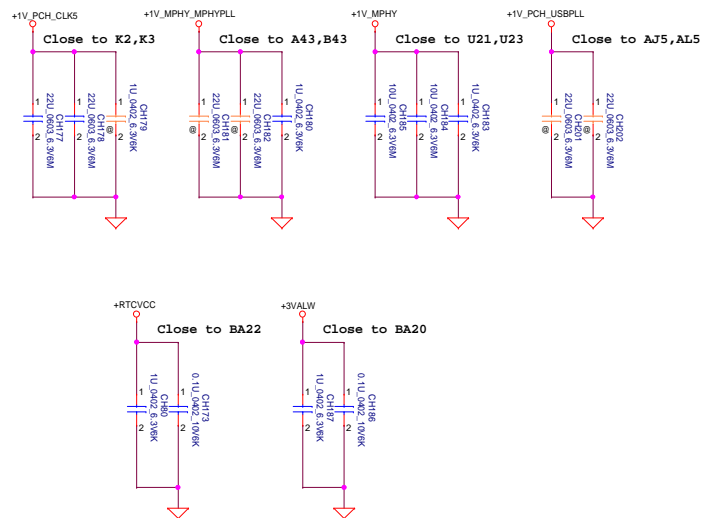


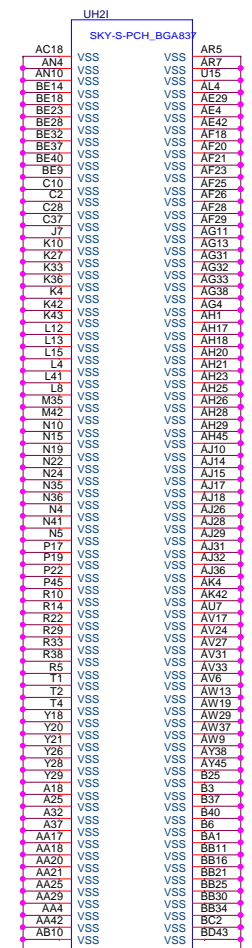
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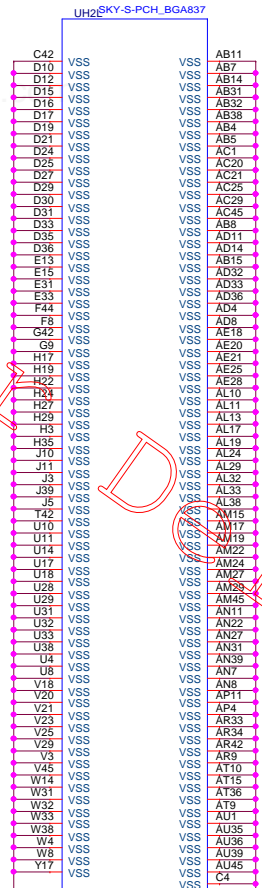
SYSTEM ID	
HIGH	14" & N16P_GT
LOW	15" & N16P_GX



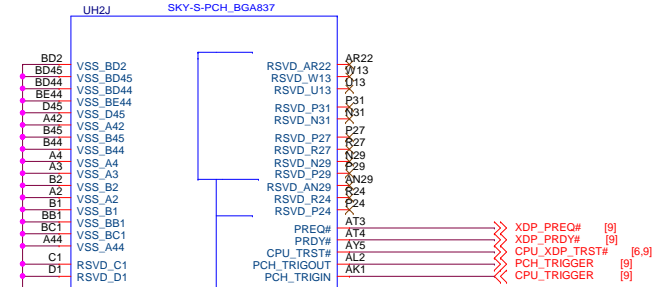




SKY-H-PCH_BGA837
REV = 1.3 9 OF 12
@

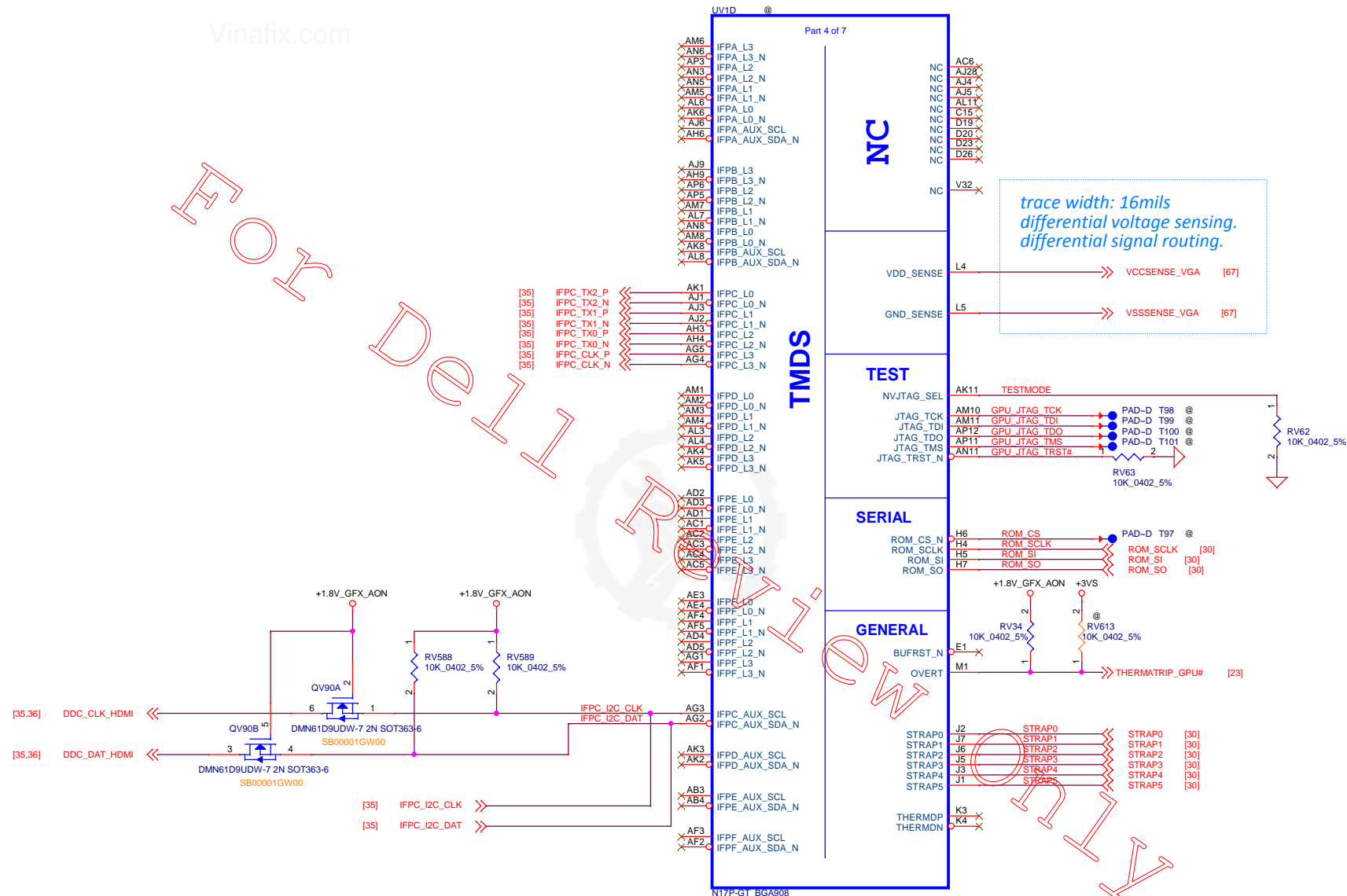


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12 OF 12 REV = 1.3
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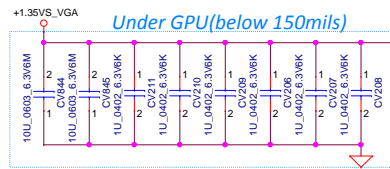
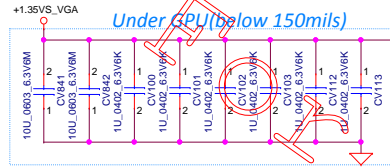
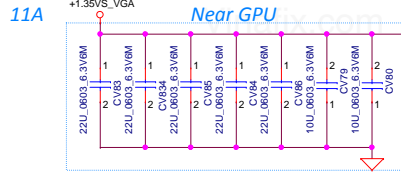


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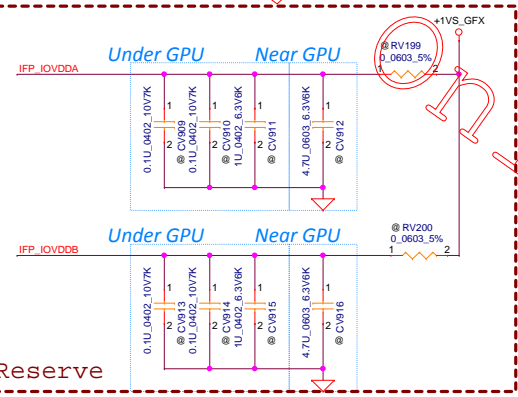
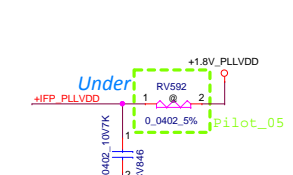
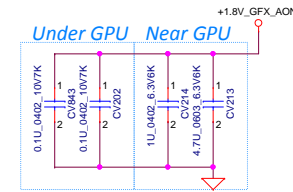
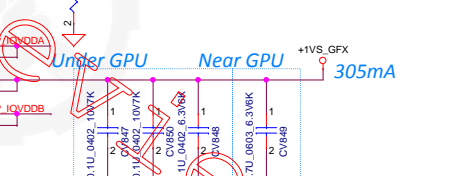
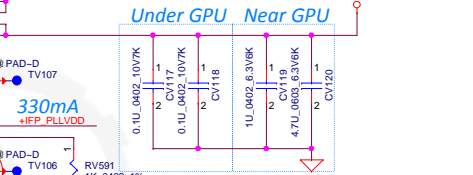
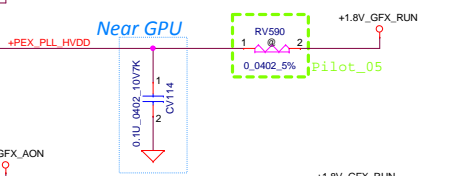
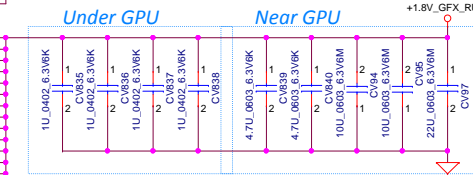
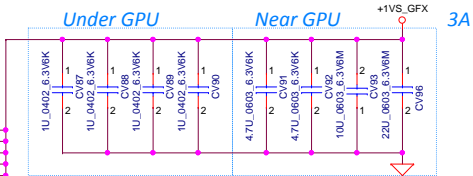
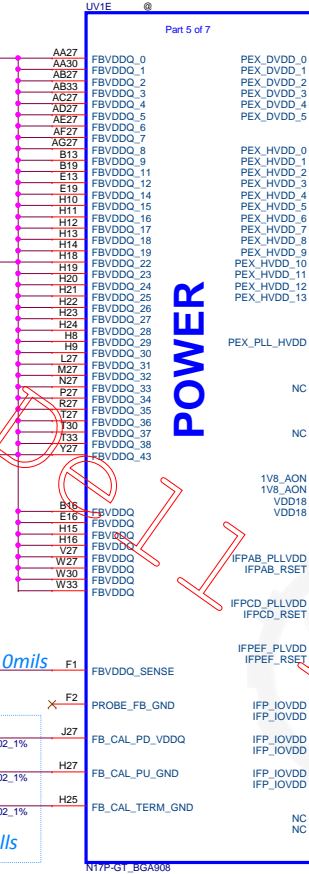
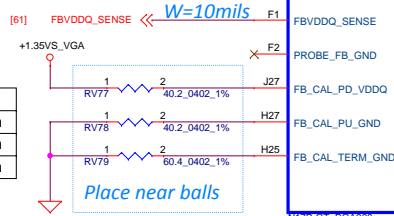




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CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm



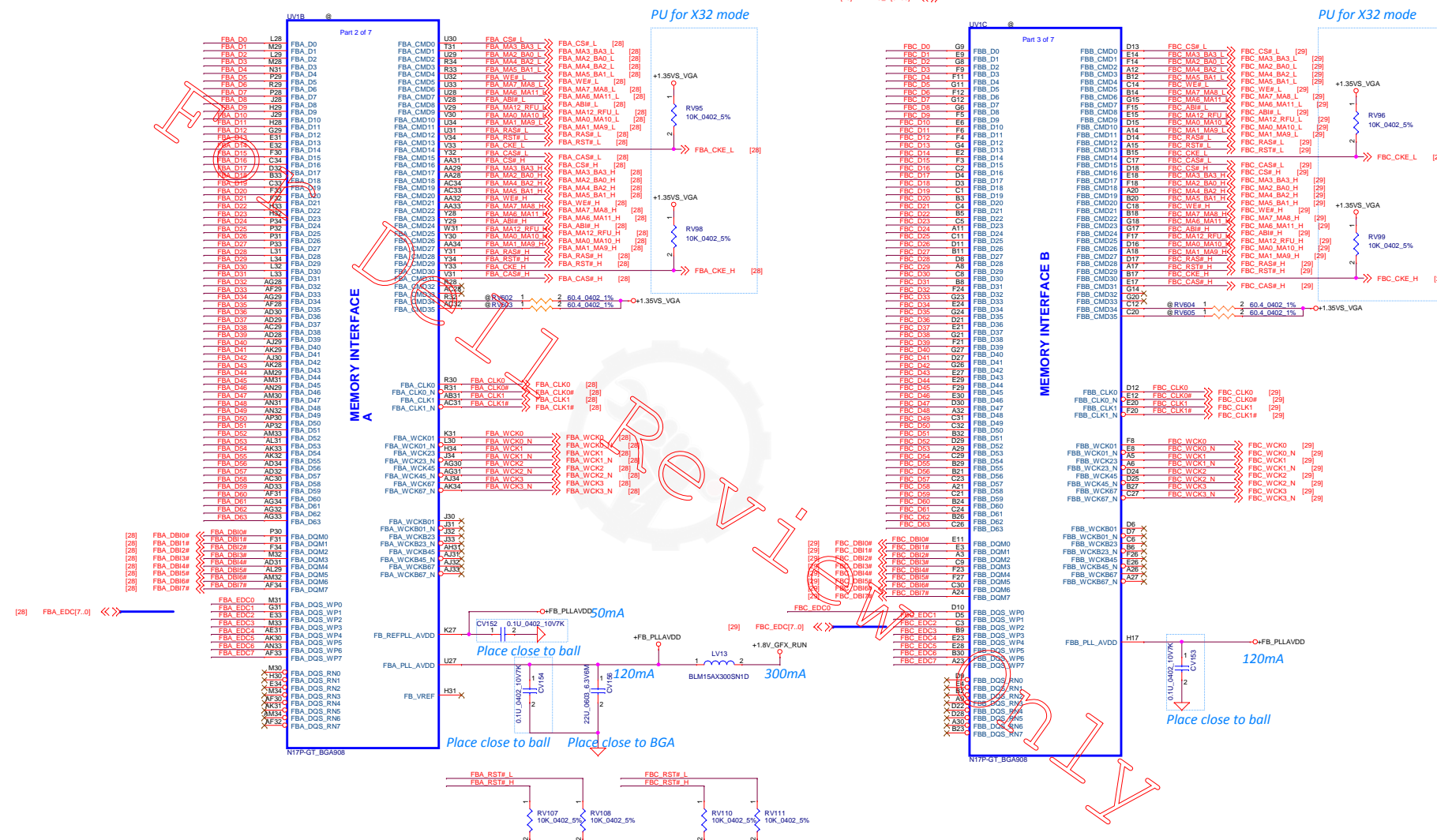


Review Only

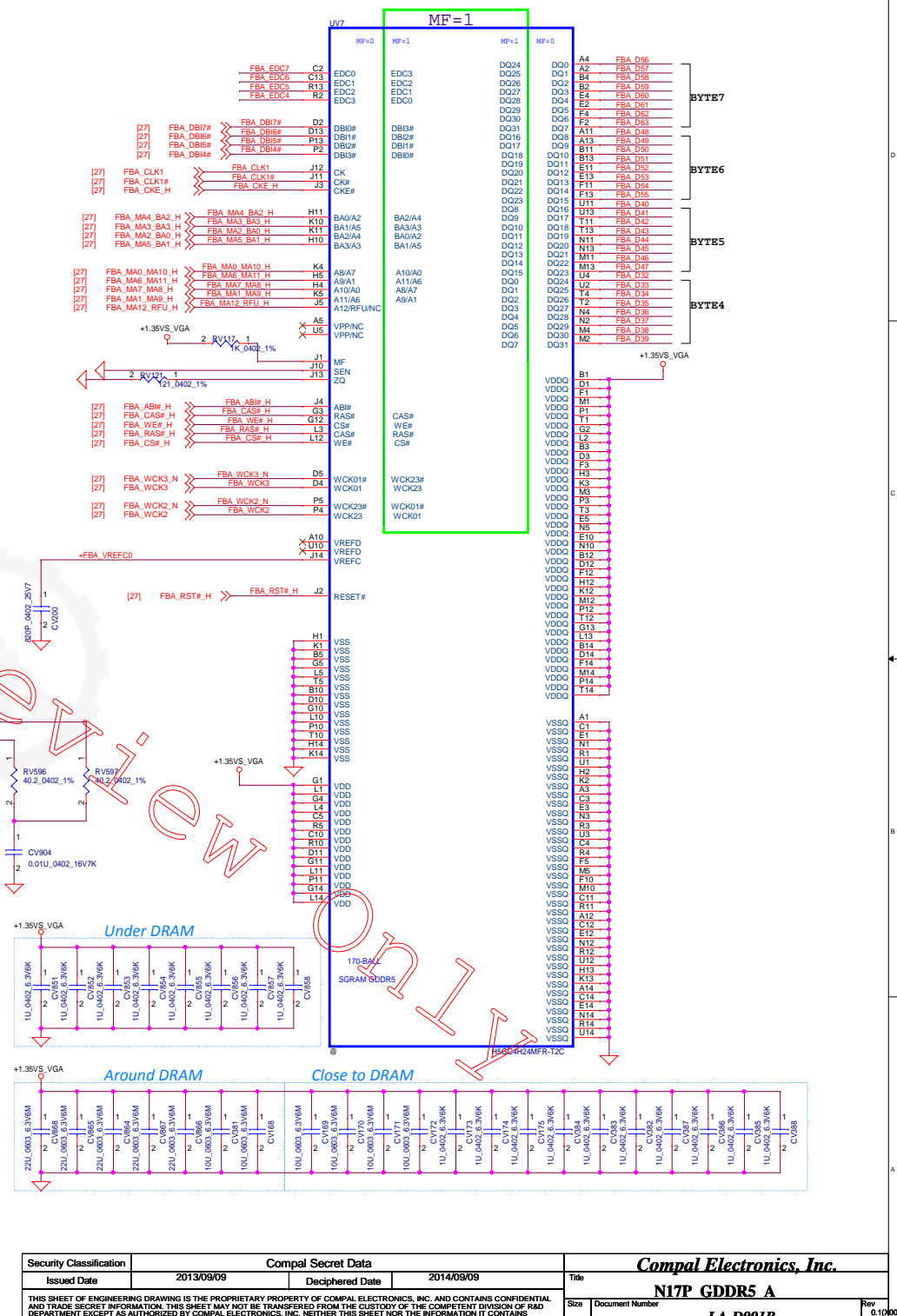
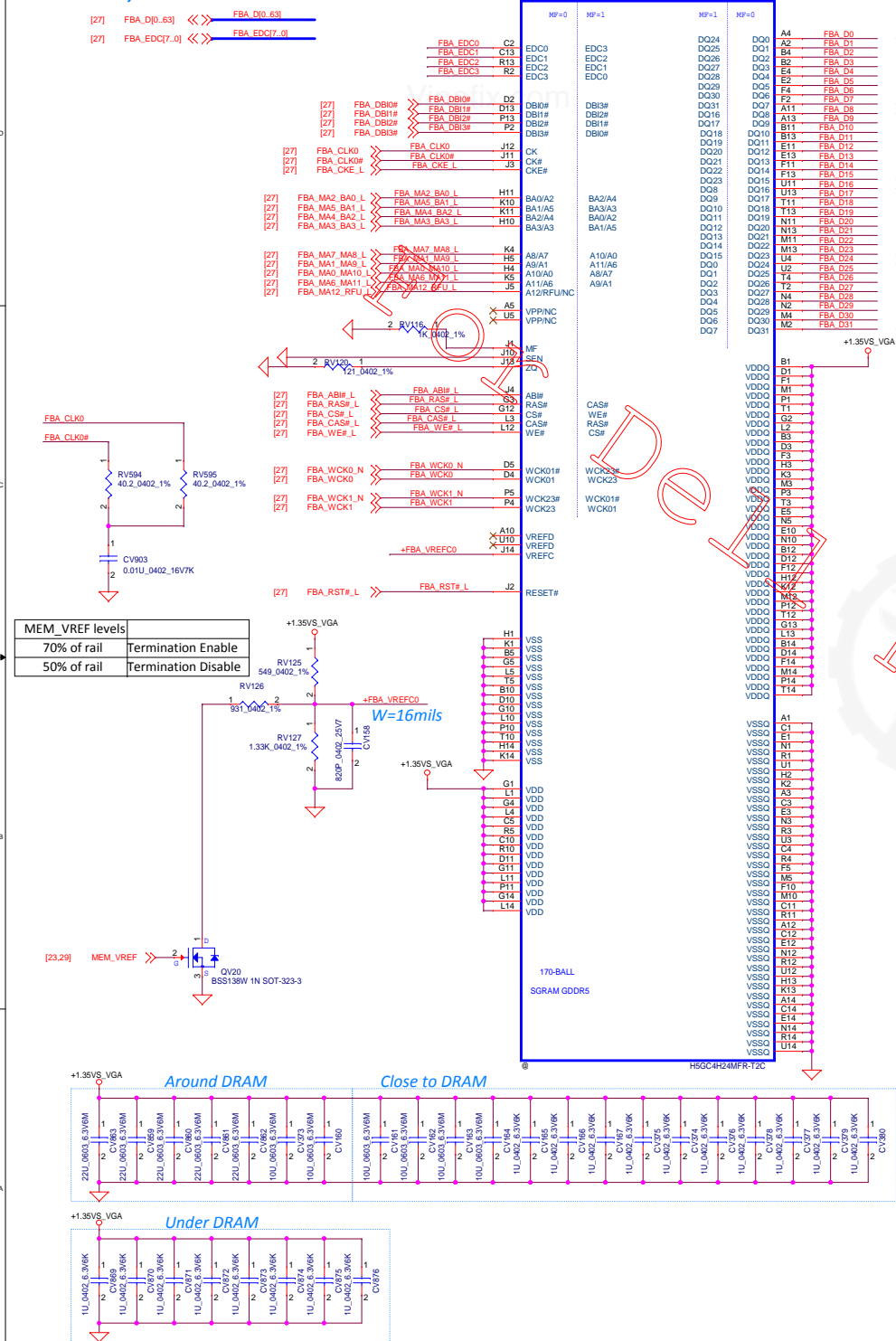
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				LA-D991P	
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FBA_D[0..63] <<> FBA_D[0..63]

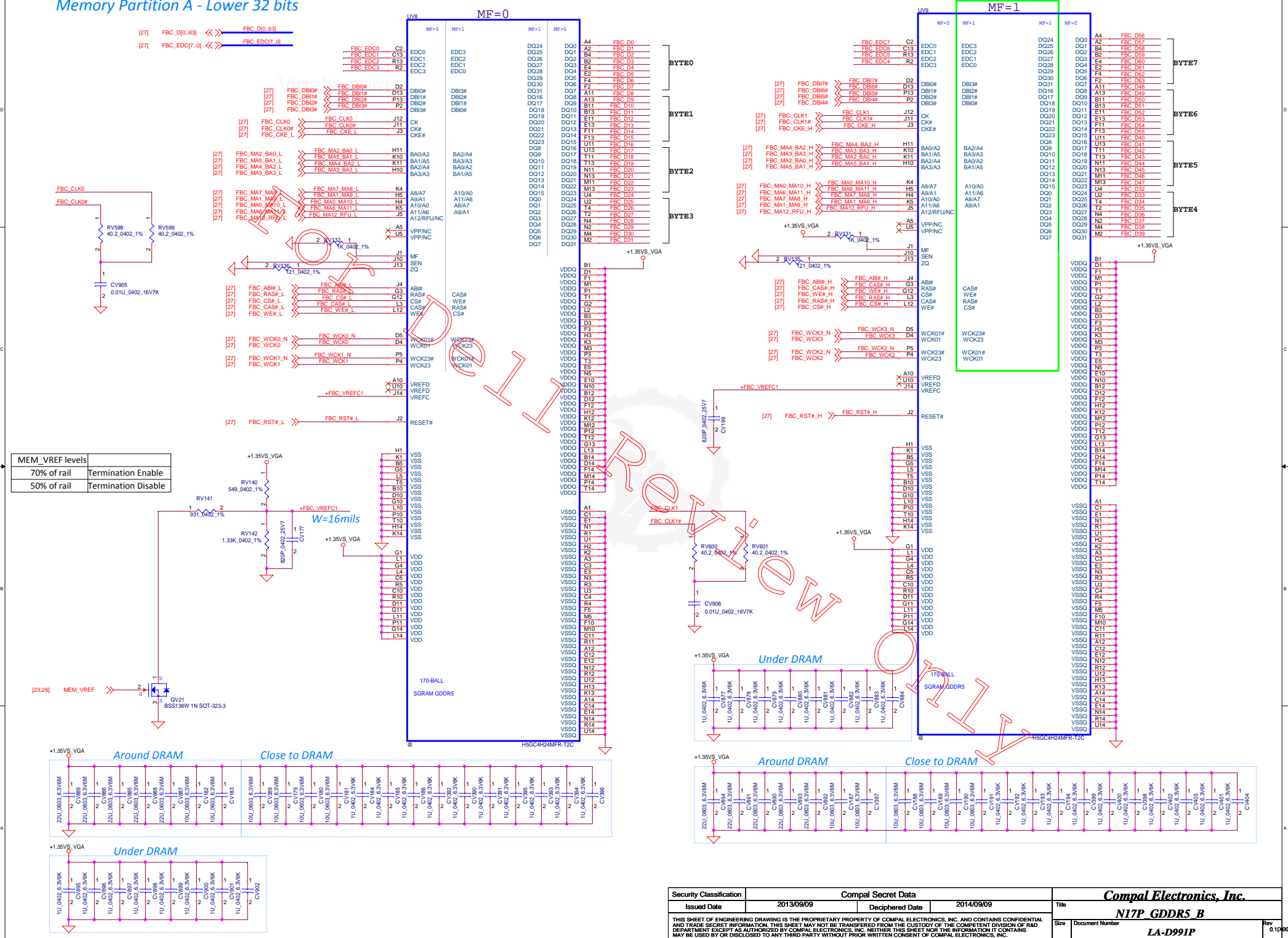
FBC_D[0..63] <<> FBC_D[0..63]

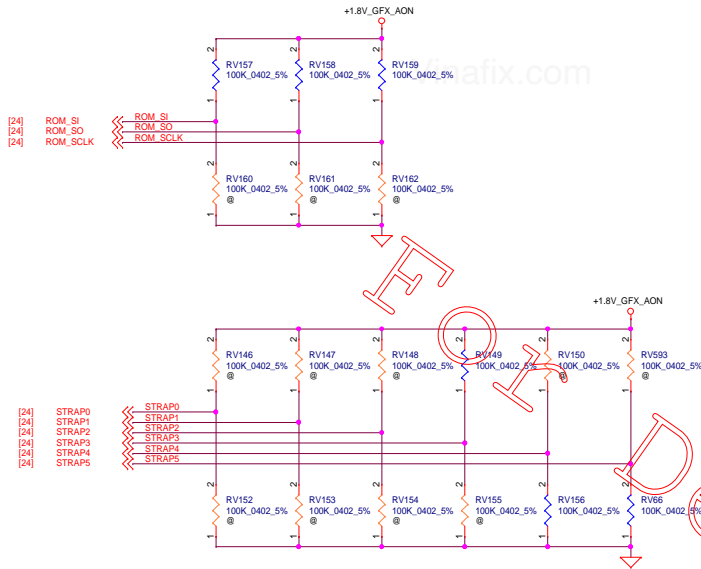


Memory Partition A - Lower 32 bits



Memory Partition A - Lower 32 bits





SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 1. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.5V/ 1.5V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	0x0	3500	N/A	Production candidate
				Micron	MT51J256M32HF-70-A	A-die	0x1	3500	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R0C	M-die	0x2	3500	N/A	Post-production candidate

Note:

1. For N17P-Gx, the maximum allowable memory case temperature is 85 °C.

2. N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

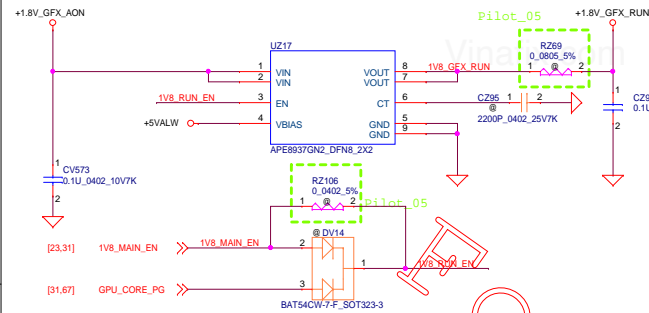
Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
8	H	H	H	ENABLED	disabled	disabled	disabled

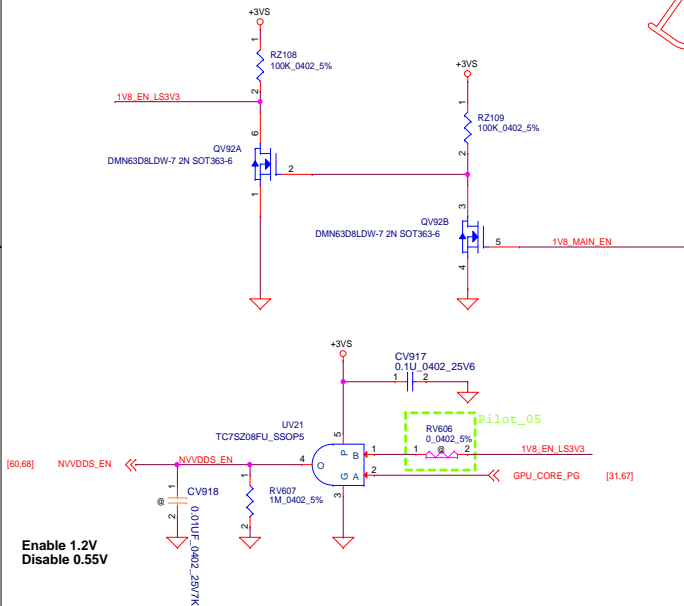
Total Display Links (HDMI, DP or DVI)			See This Row of Table 5.5			
Total Enabled for Audio (HDMI, DP or DVI)			Is eDP Supported on:			
			IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
1	1	--	--	--	--	8

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Size C	Document Number	LA-D991P		Rev 0.1/000
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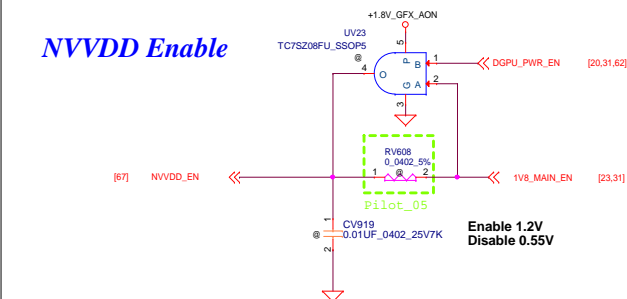
+1.8V_GFX_RUN



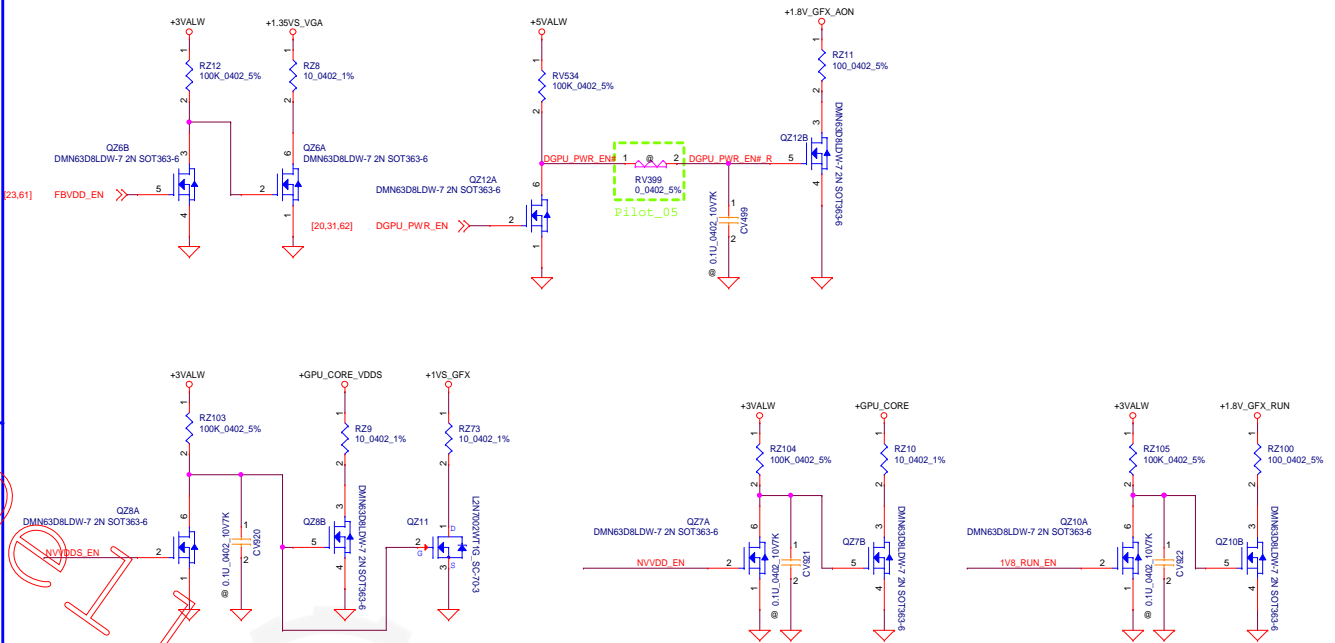
NVVDSS Enable



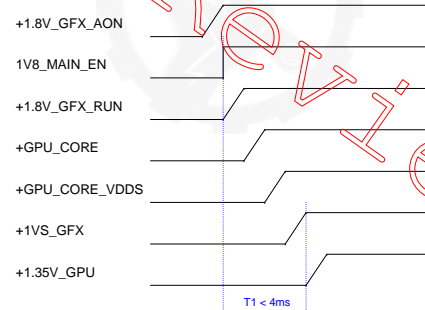
NVDD Enable



Discharge

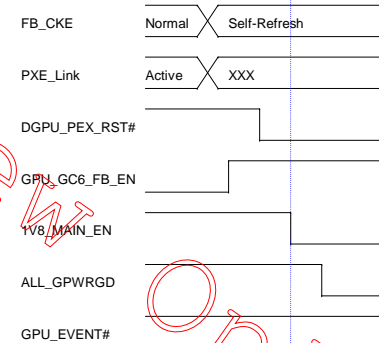


GPU Power Up Sequence



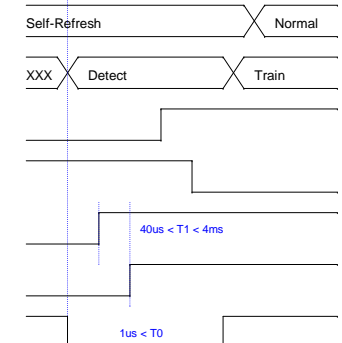
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

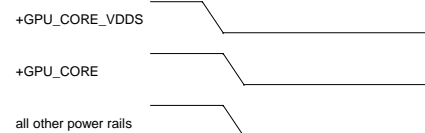


The entire entry/exit sequence must complete within 200 ms.

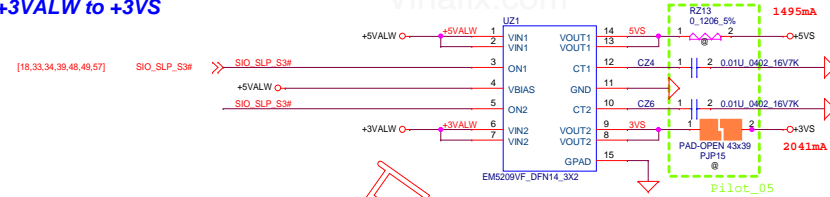
GPU GC6 Exit Sequence



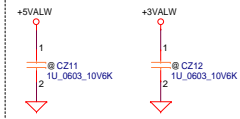
GPU Power Down Sequence



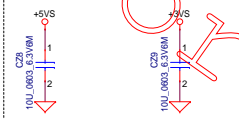
+5VALW to +5VS
+3VALW to +3VS



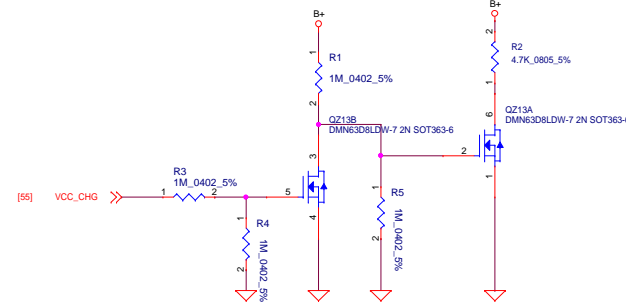
Close UZ1



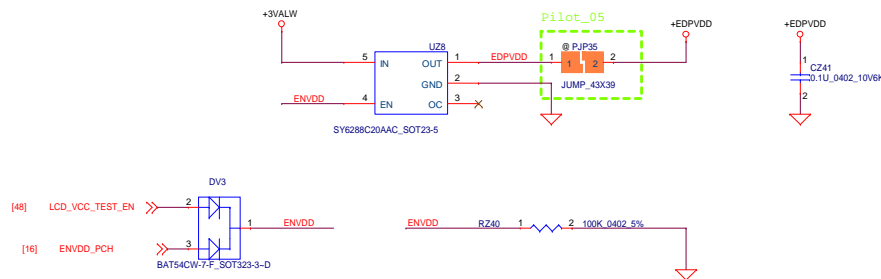
Close UZ1



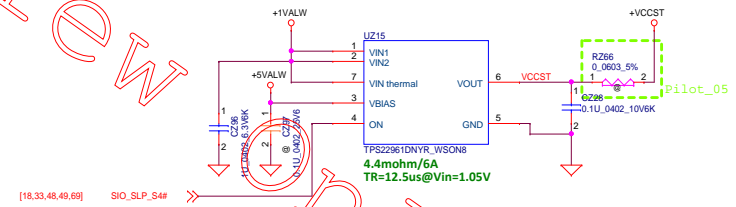
B+ Discharge



eDP & Camera Load Switch

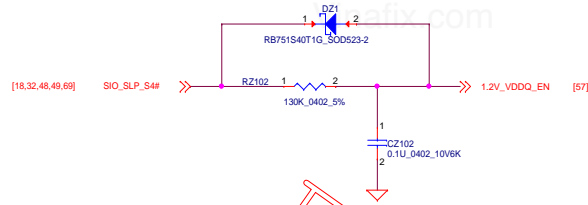


+VCCST Load Switch

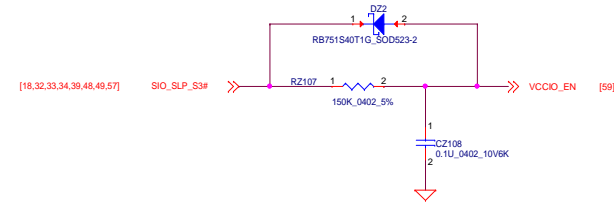


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				Date: Tuesday, November 08, 2016 Sheet 32 of 70

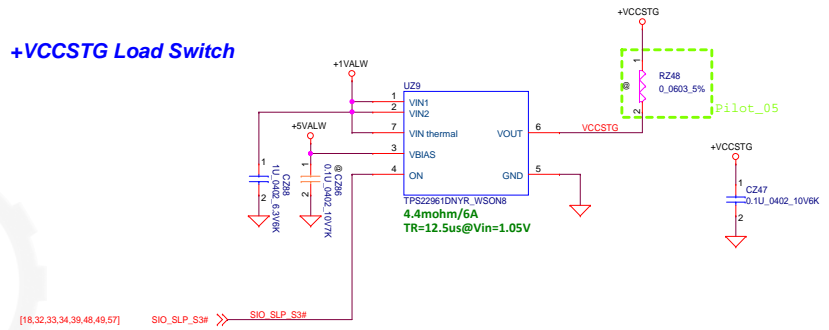
+1.2V_DDR Enable



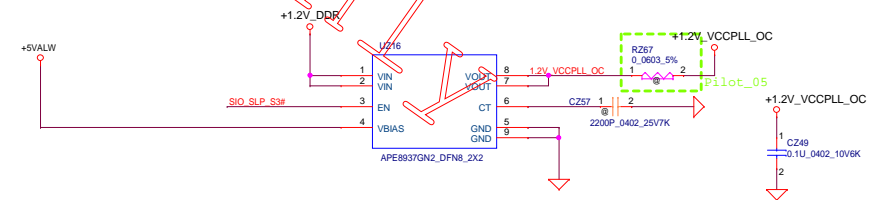
+VCCIO Enable



+VCCSTG Load Switch

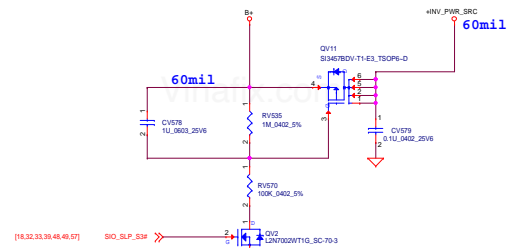


+VCCPLL_OC Load Switch

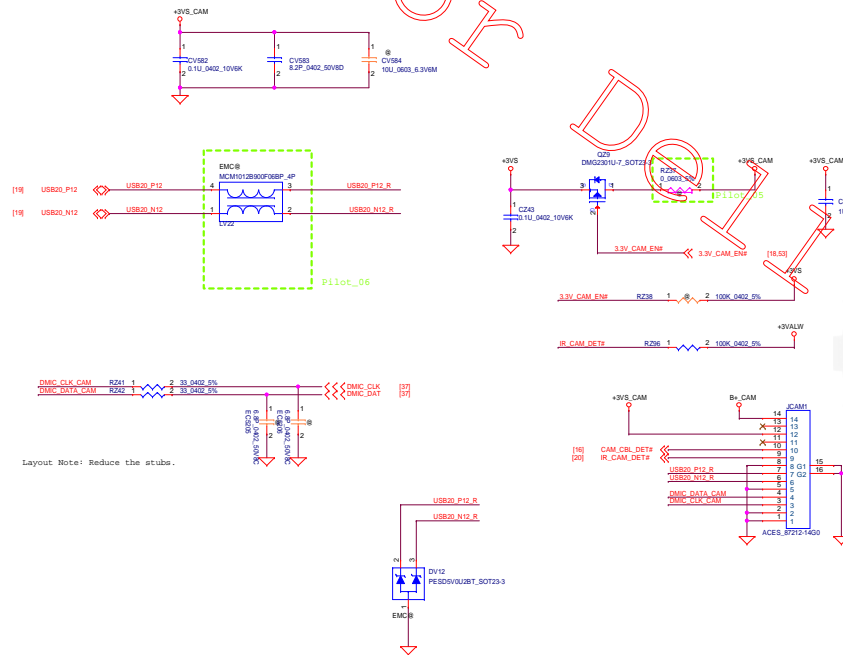


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		Date	LA-D991P
		Sheet	33 of 70

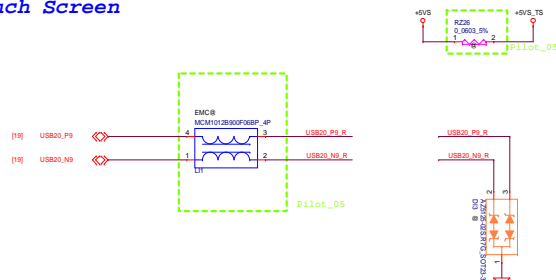
LCD backlight PWR CTRL



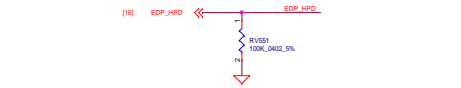
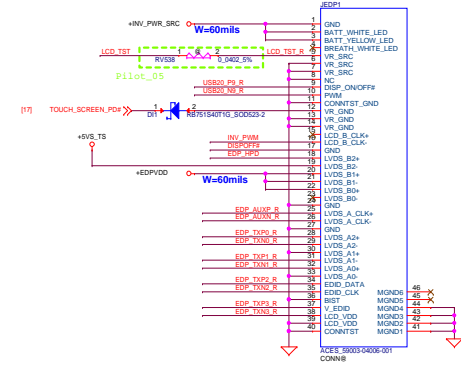
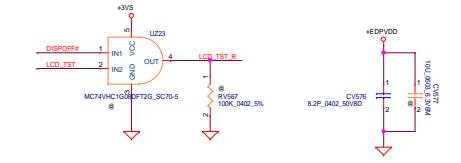
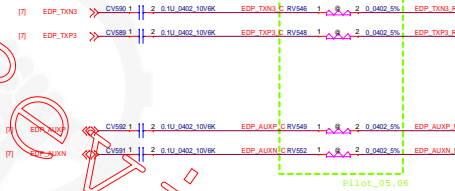
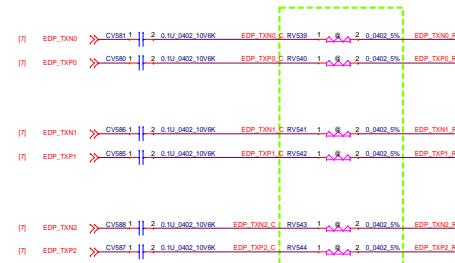
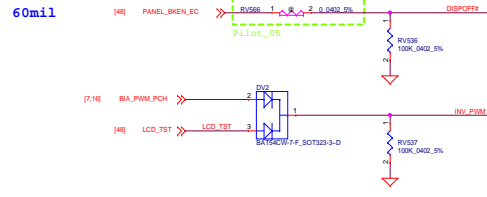
CCD +DMIC Conn.



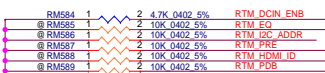
Touch Screen



eDP & TS Conn.



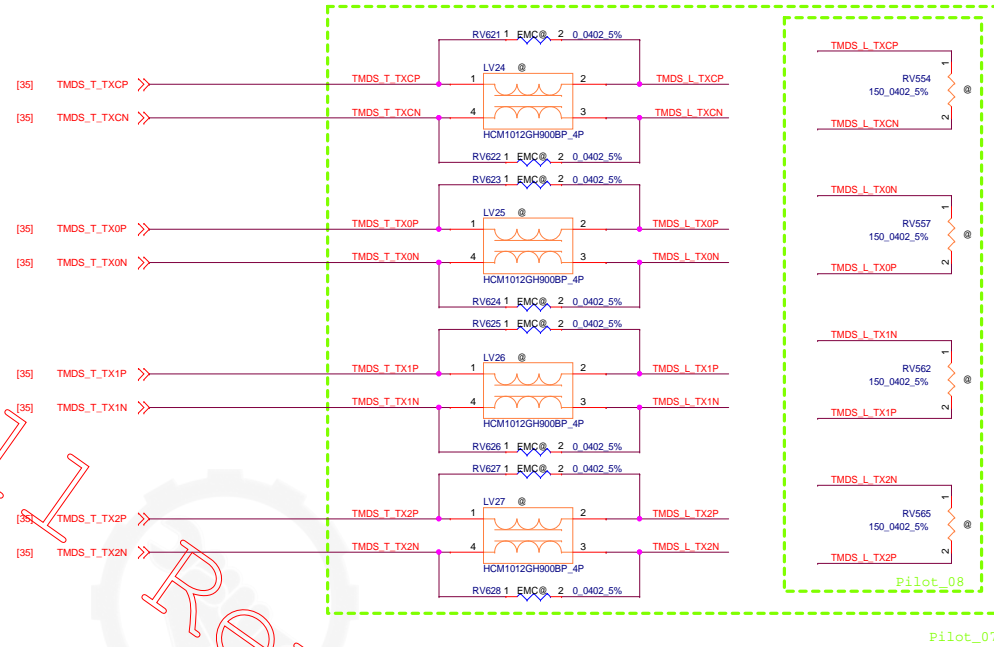
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	eDP TS conn.
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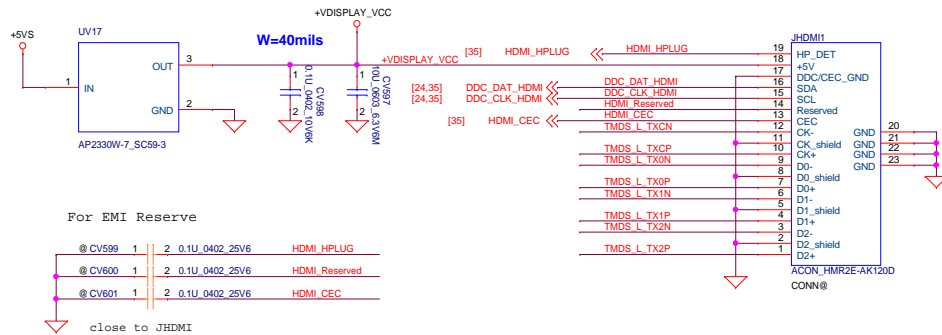
Vinafix.com

Place close to JHDMI1

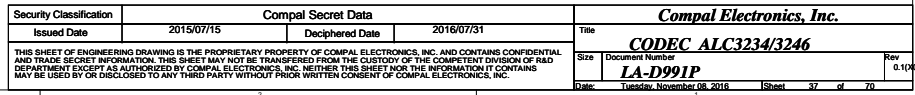
Place between ESD and CM-Choke



HDMI conn



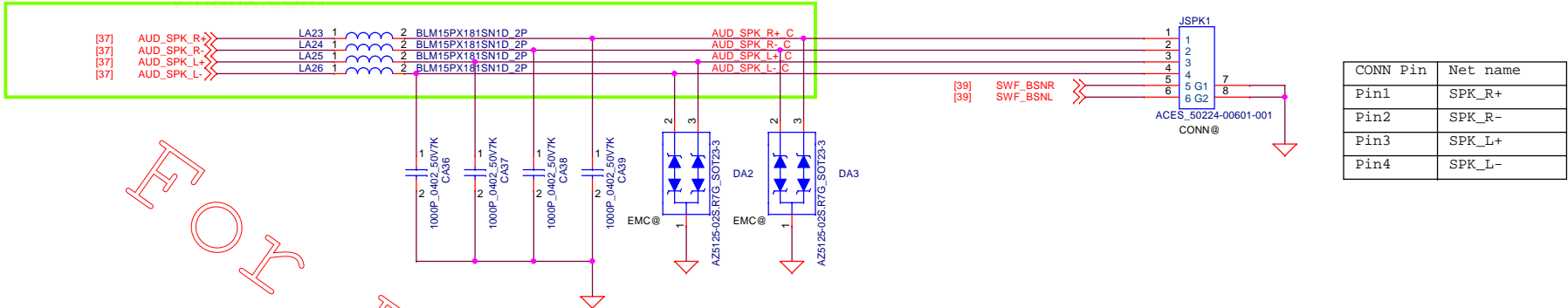
Security Classification	Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Compal Electronics, Inc.
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Size	Custom	Document Number	LA-D991P	Rev 0.1/000
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Main Func = Audio

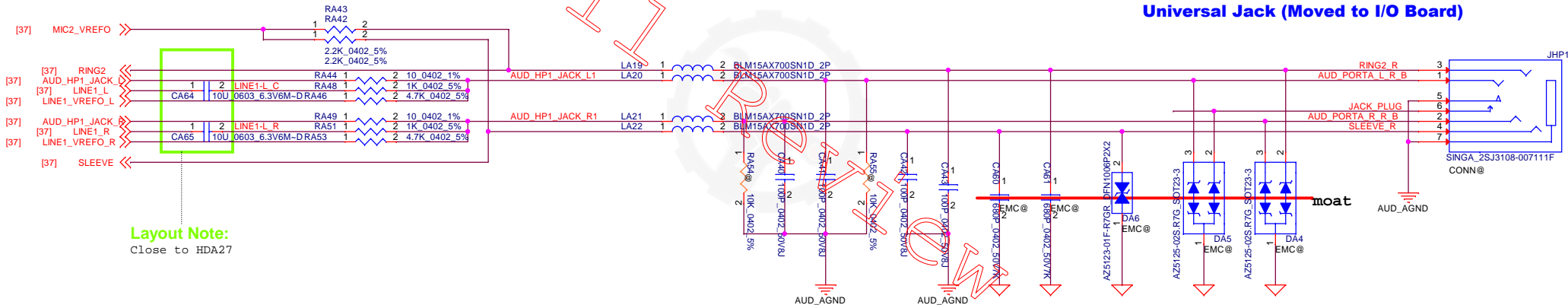
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)

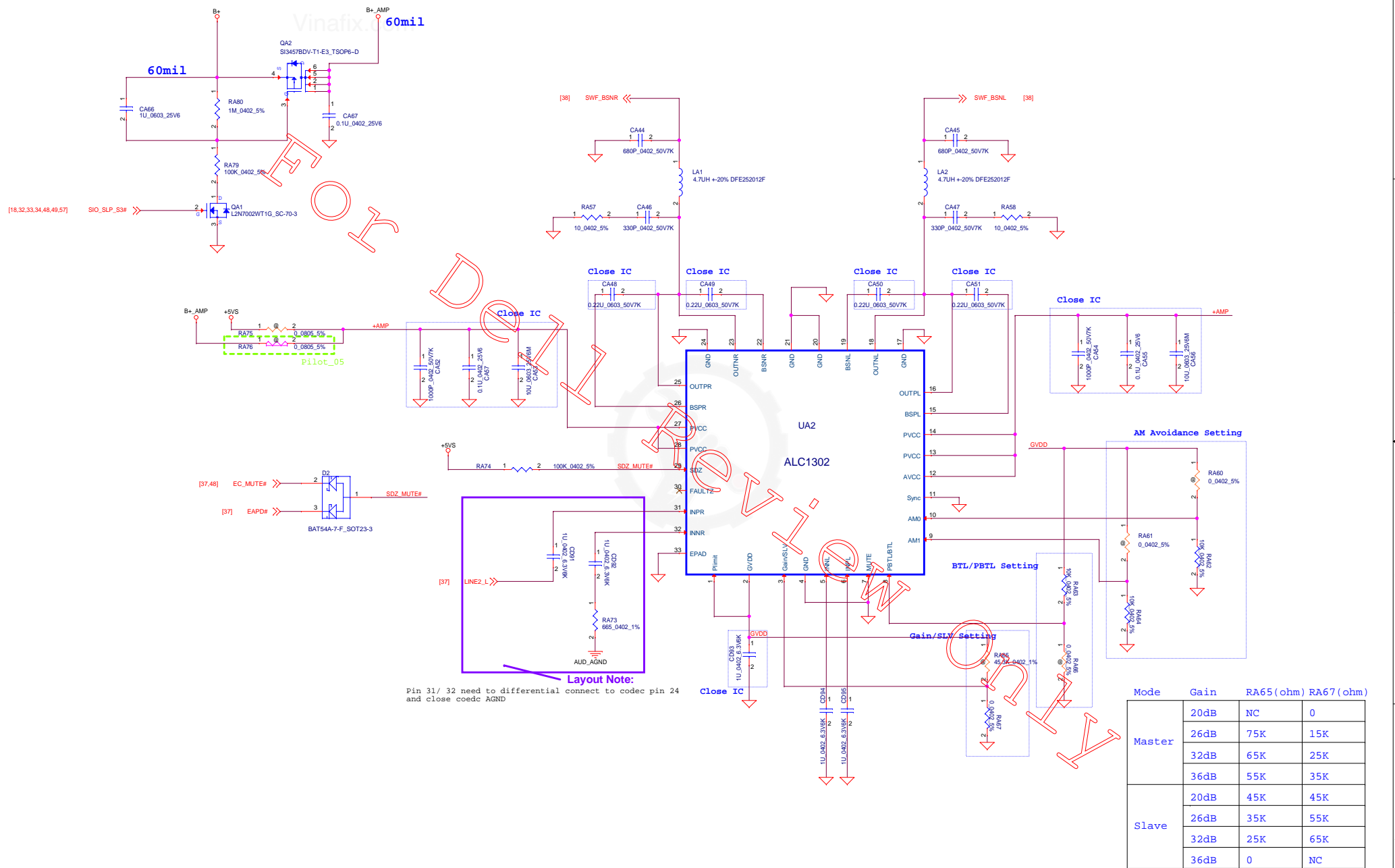


Layout Note:
Close to HDA27

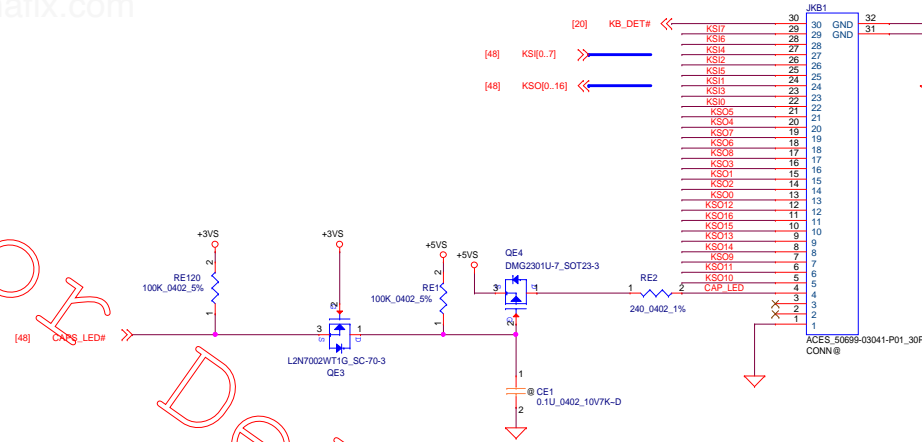
JACK_PLUG 10 mils RA56 1 @ 2 0 0402 5% 10 mils >>> AUD_SENSE [37]
Pilot_05

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Issued Date	2015/07/15	Deciphered Date	2016/07/31	Title	SPKR/JACK	
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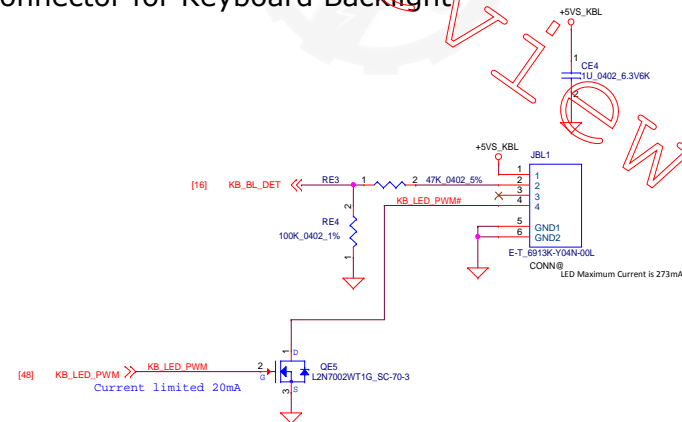
Subwoofer AMP



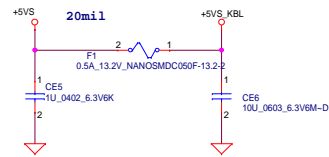
Connector for Keyboard



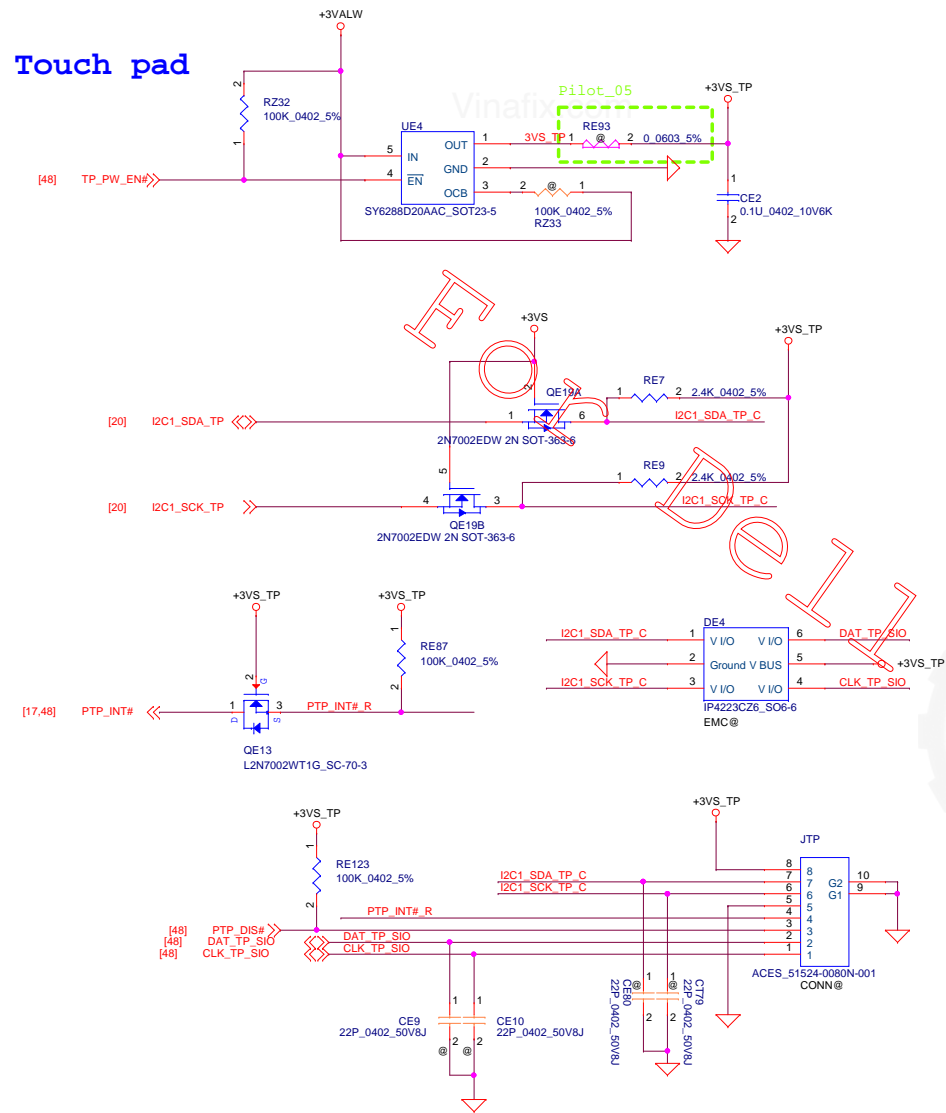
Connector for Keyboard Backlight



Fuse for Backlight

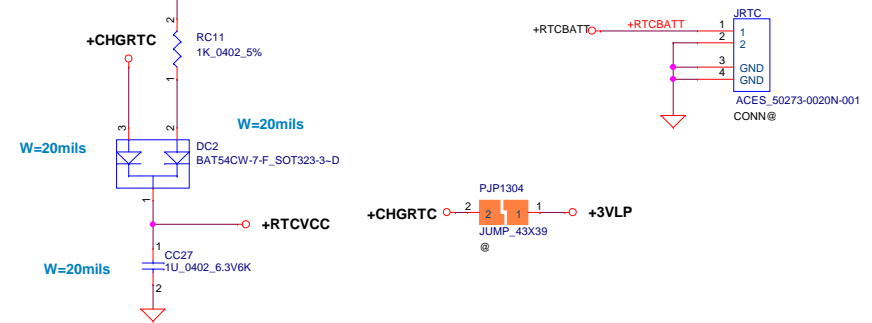


Touch pad

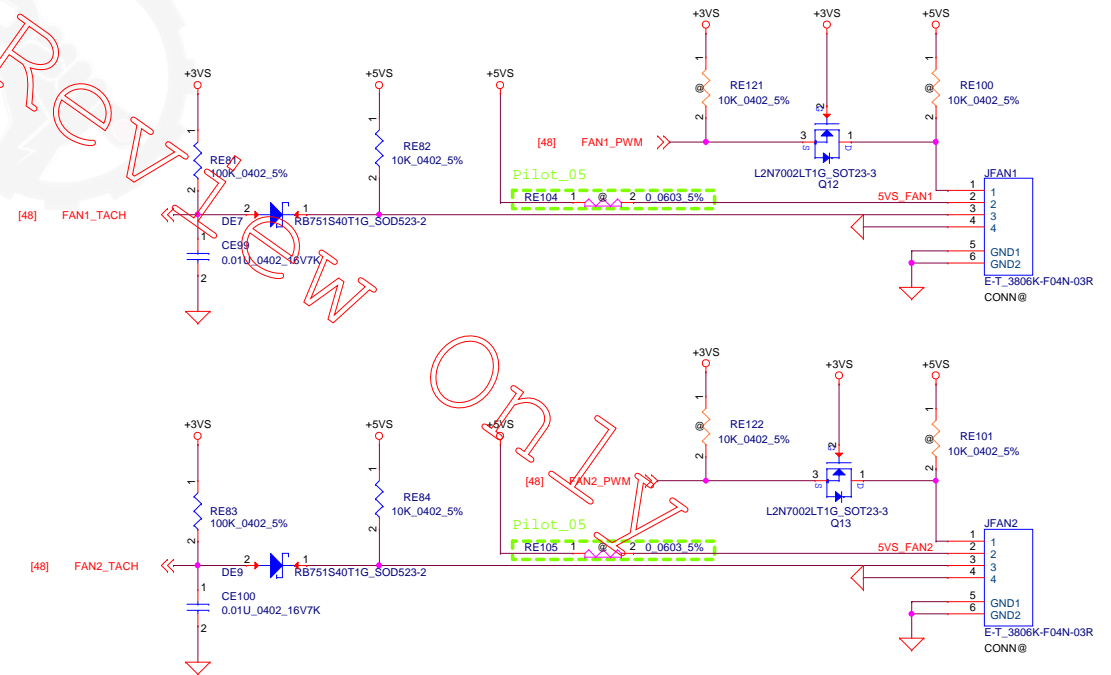


RTC Battery non- Charge Function

RTC Battery +RTCBATT



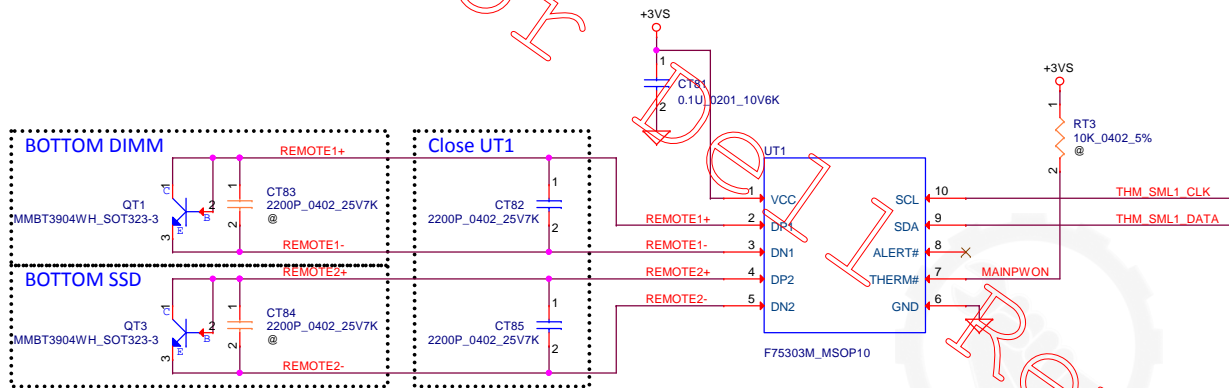
PWM FAN



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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	FAN/TP/KB/PWR SW
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Vinafix.com

Fintek thermal sensor
placed TOP near between GPU & CPU

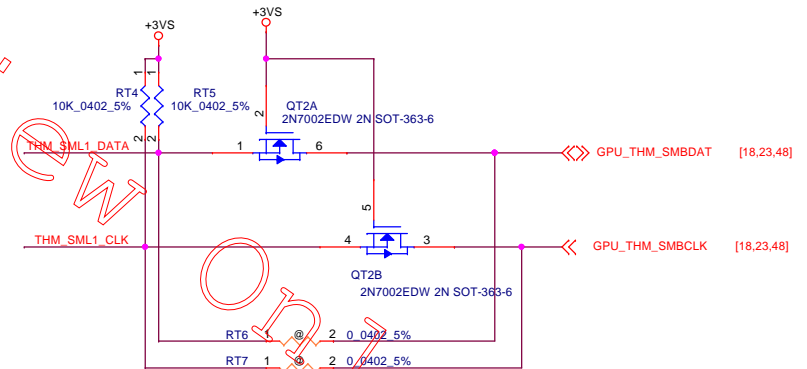
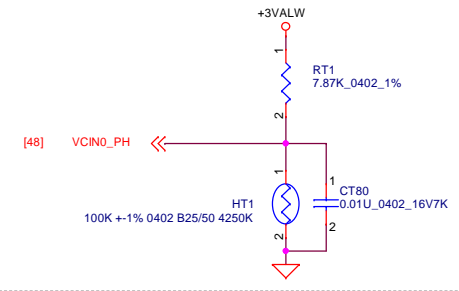


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

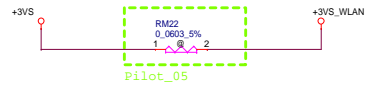
2nd source
SA000029210-->EMC1403-2-AIZL-TR

CPU TOP side

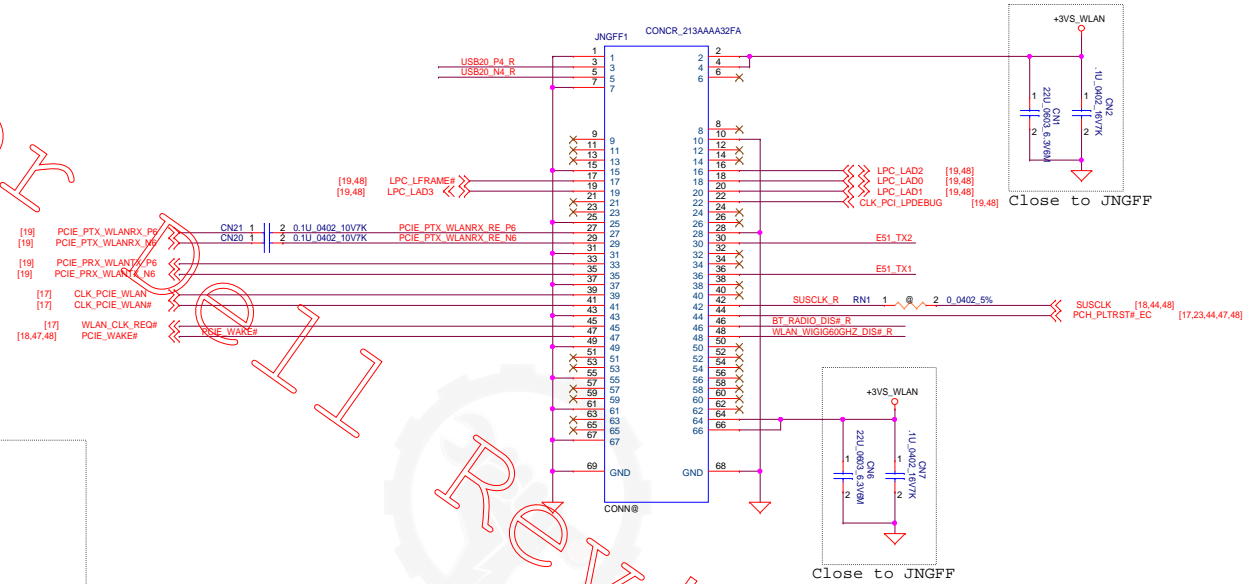
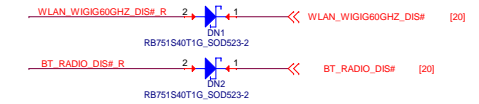


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								Size		Document Number		Rev	
								LA-D991P		0.1(00)			
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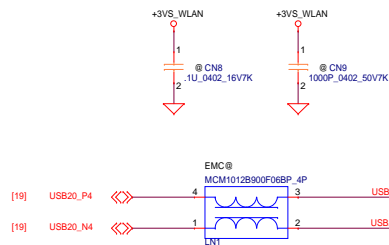
M.2 Slot-A Key-A (WLAN + BT)



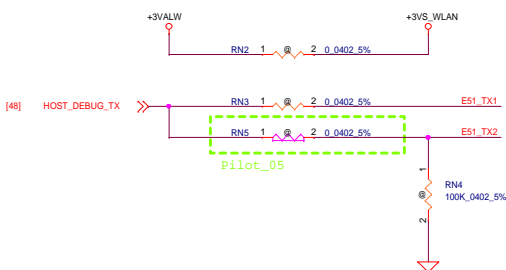
Vinafix.com



Reserve for EMI



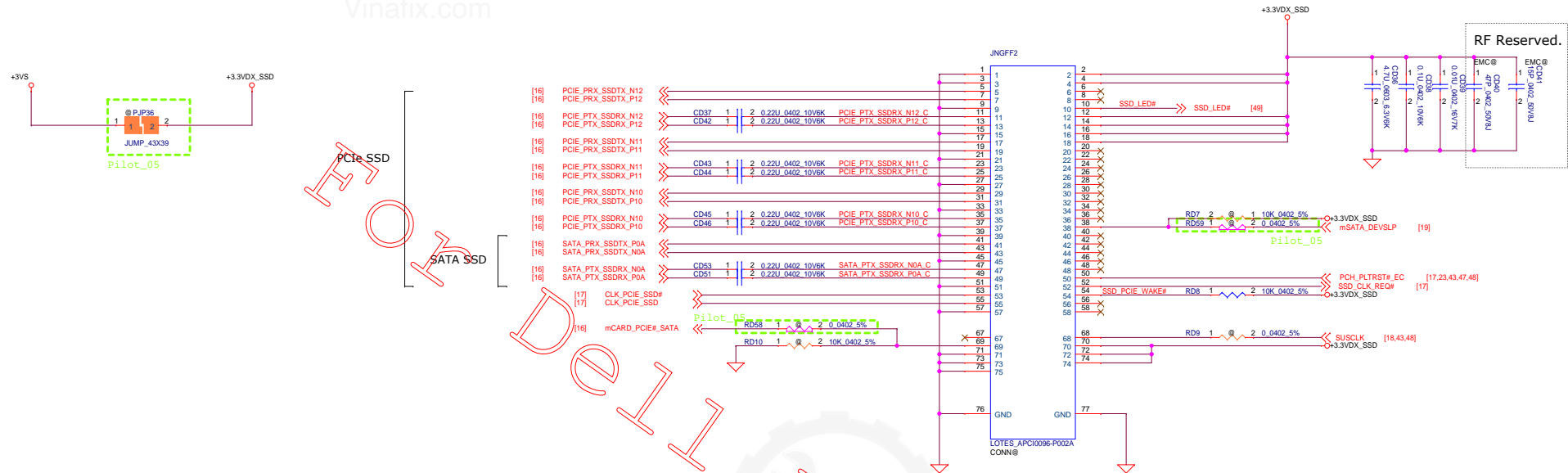
Reserve for NGFF Debug Card



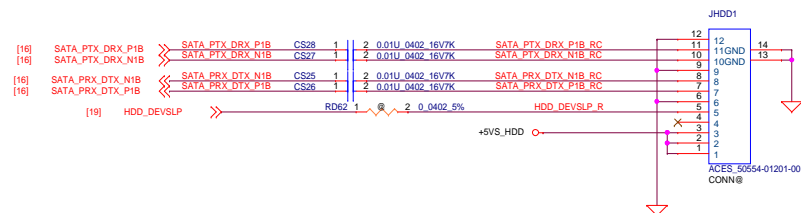
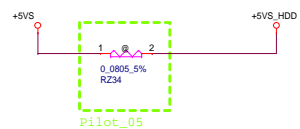
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
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Size	C	Document Number	LA-D991P	Rev
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M.2 Slot-C Key-M (SSD)

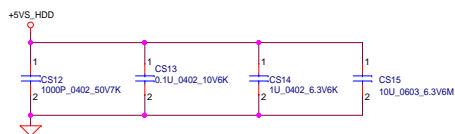
Vinafix.com



HDD CONN



Place near HDD CONN (JHDD1)

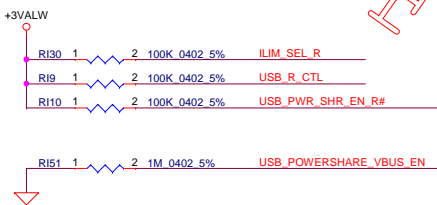


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Size C	Document Number LA-D991P	Sheet 44	of 70	Tuesday, November 08, 2016

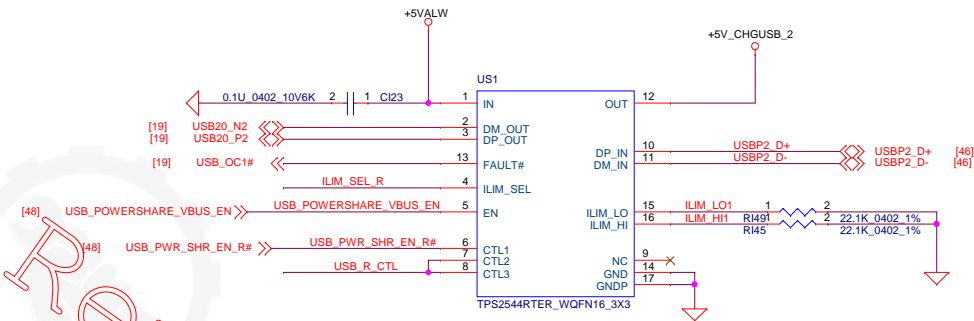
USB Powershare

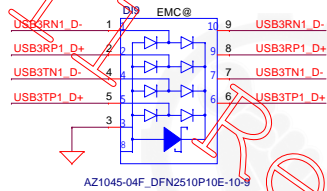
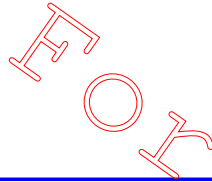
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

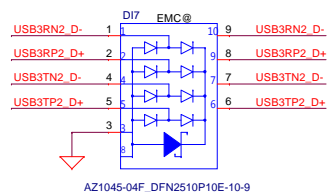


USB3.0 / USB2.0 Port1

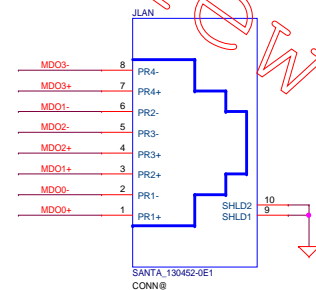
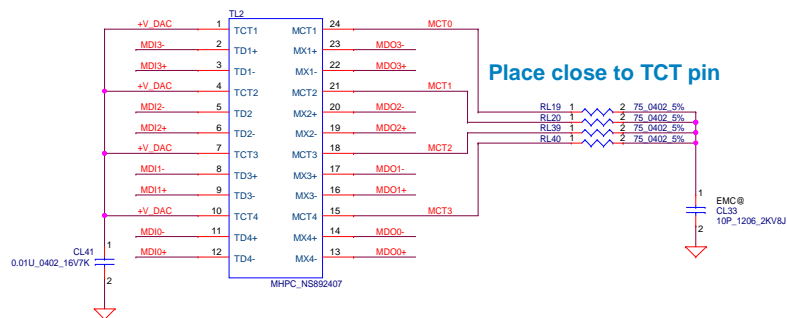
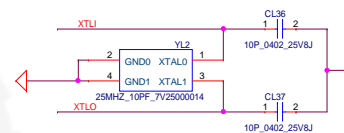
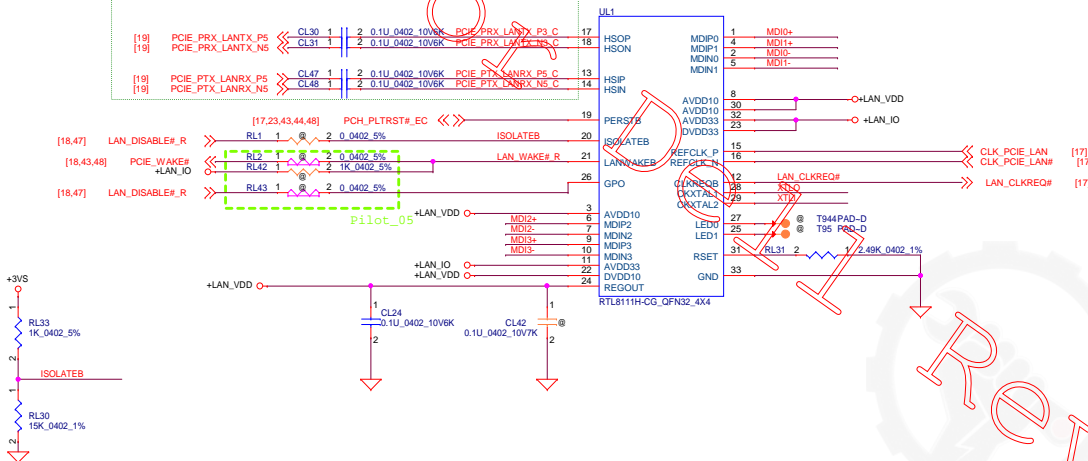
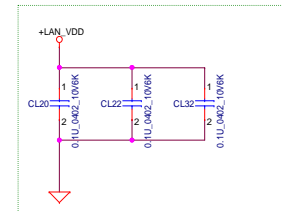
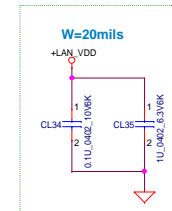
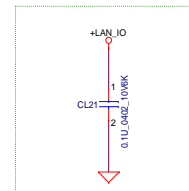
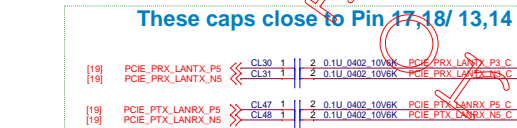
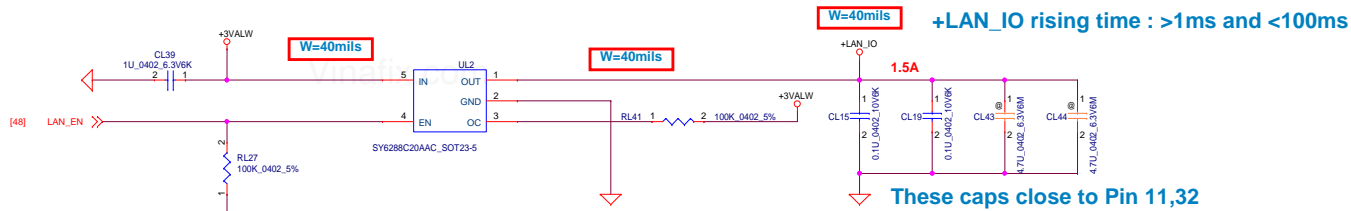


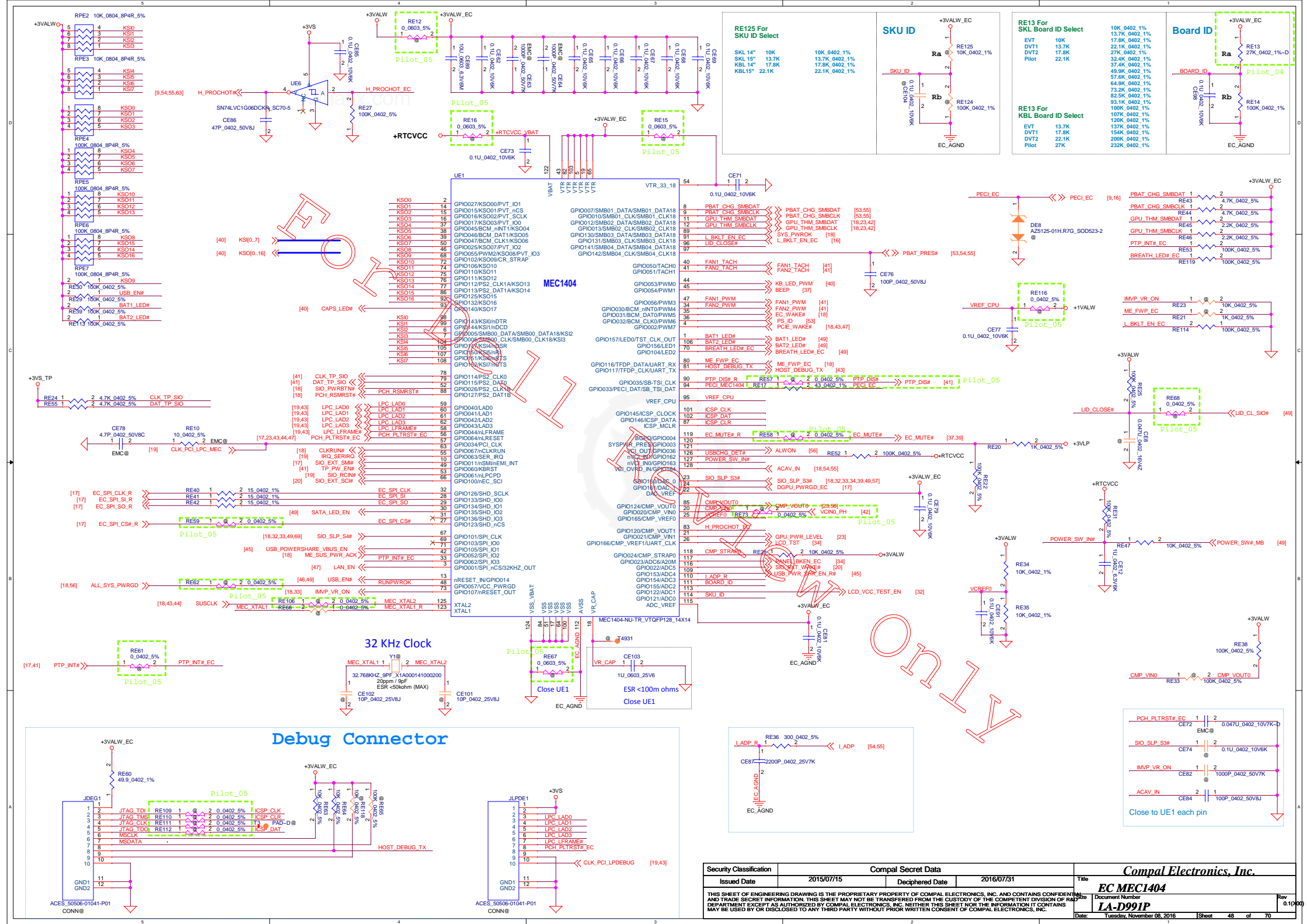


USB3.0 / USB2.0 Port1

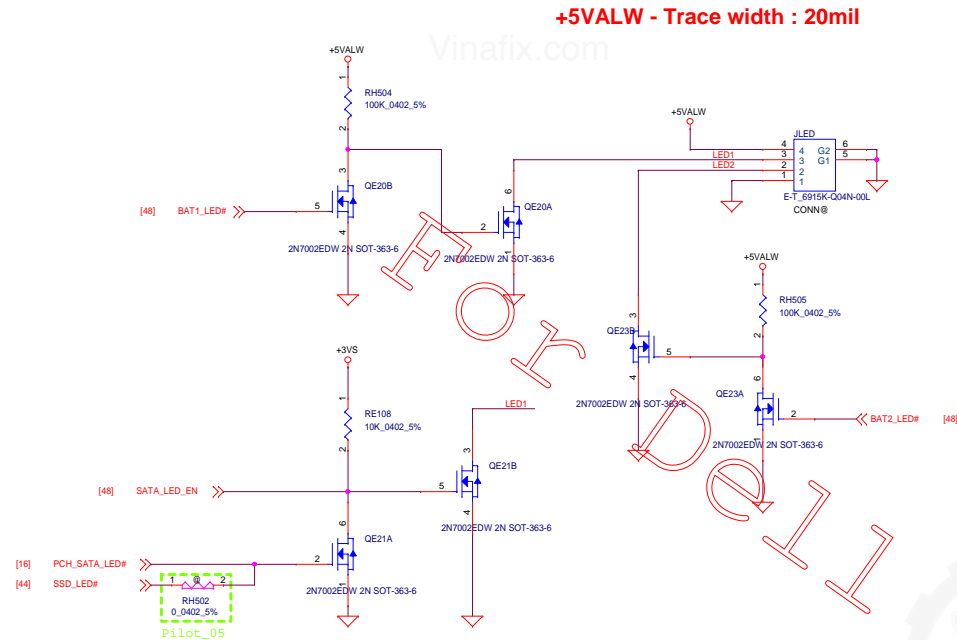
[illegible]

Rev	
0,1(200)	

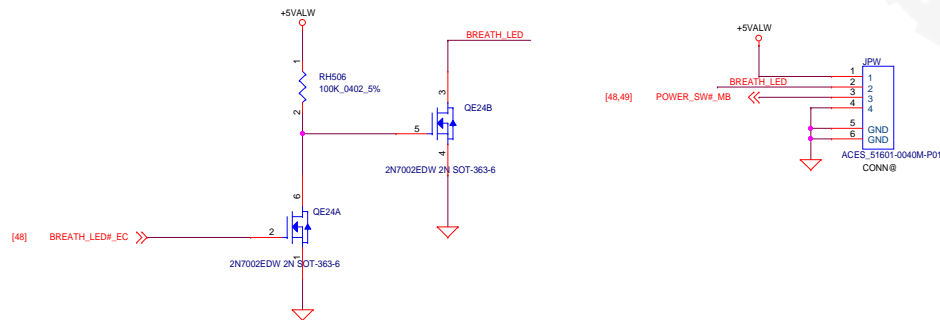




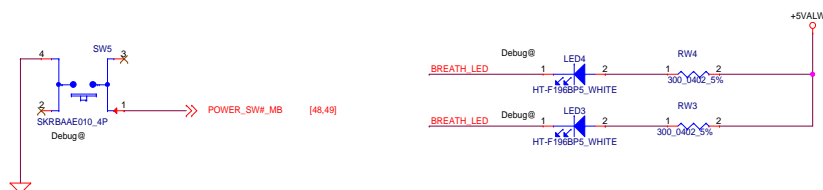
LED Board Connector



TO PWR BOARD

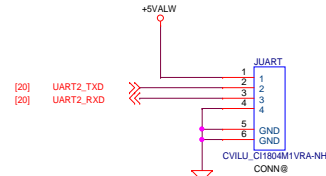


Power Button & LED (Reserve)

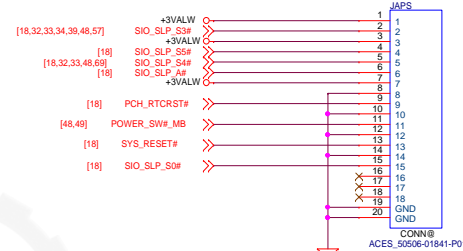


I/O & APS & UART CONN

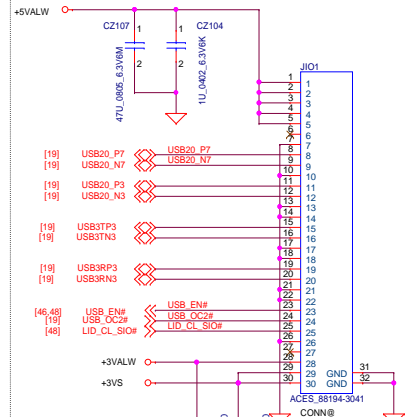
UART CONN



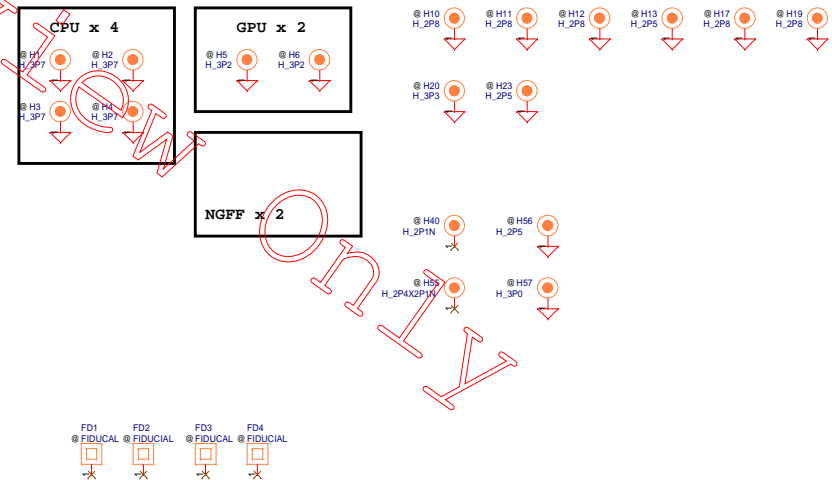
APS CONN



I/O CONN



Screw Hole

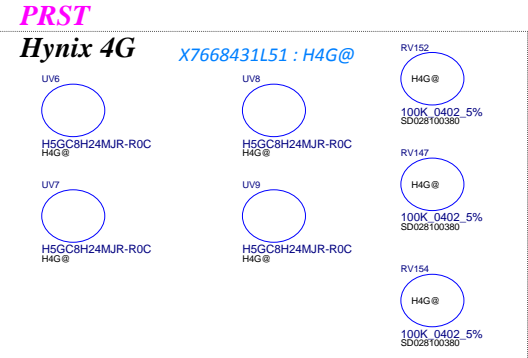
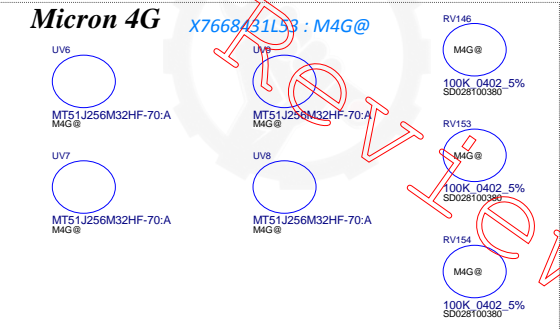
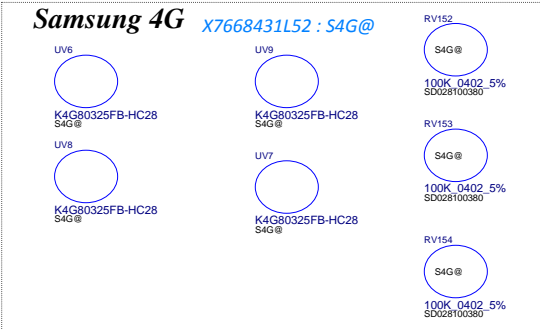
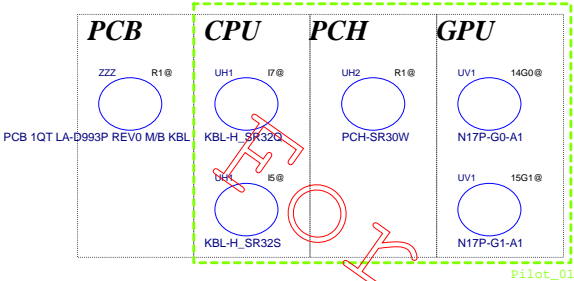


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				TPM/BTB conn.	
				Size	Document Number
					Rev
				LA-D991P	
Date:				Tuesday, November 08, 2016	
Sheet				49 of 70	

MODEL NAME : *BBV00/ BBV10*
PCB NO : *LA-D993P*

Bom Structure

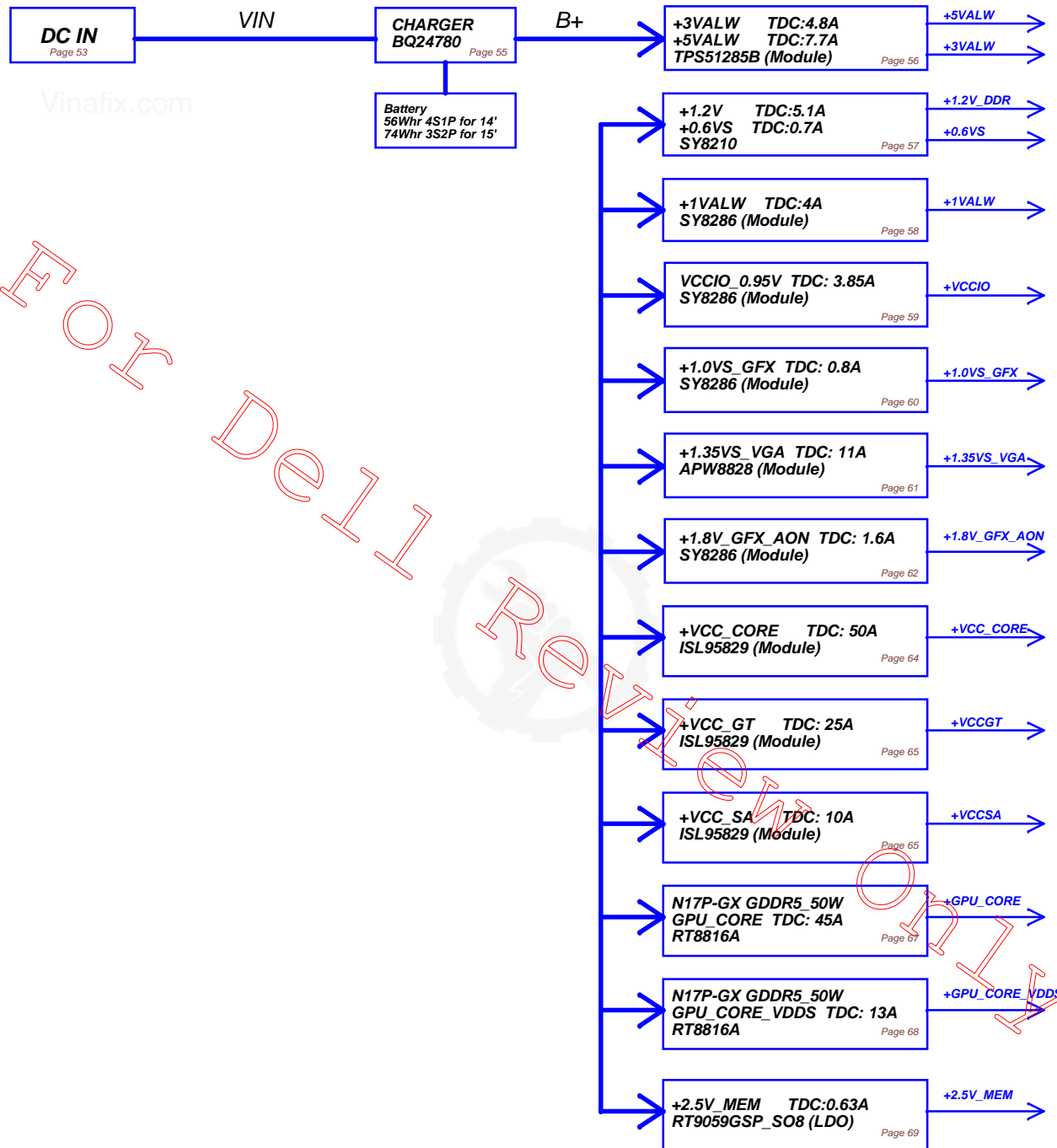
Vinafix.com



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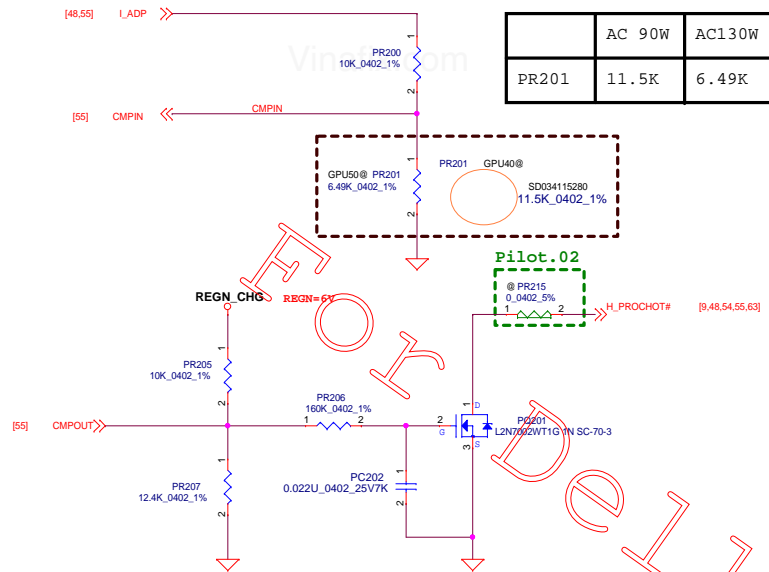
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				LA-D991P	0.1000
Date: Tuesday, November 08, 2016				Sheet	51 of 70

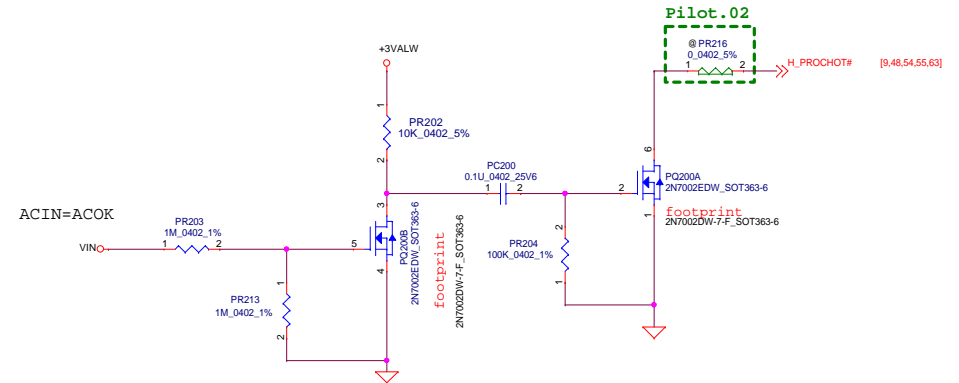


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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Power Block Diagram
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				LA-D993P	Rev 01000
				Date	Thursday, November 08, 2018
				ISect	82 of 70

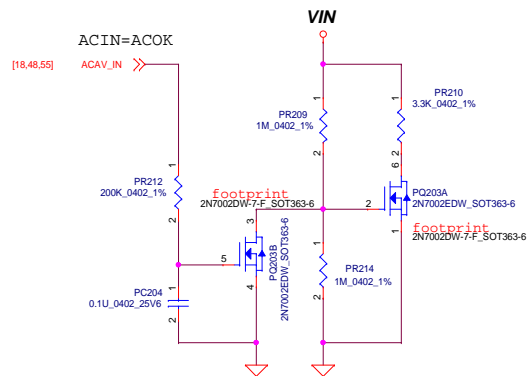
When CMPIN> Vref(2.3V/1.3V)
CMPOUT=floating



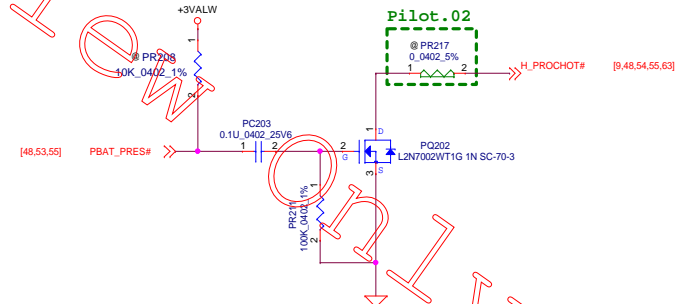
ENG0012879 Circuit-1
Delay Adapter OC H_PROCHOT# 2ms while
Hybrid power transition



Ref ENG0012879 Circuit-2
HW Asserts H_PROCHOT# when ac adapter
is being unplugged and keep low for 10ms
until SW prochot# is issued by EC

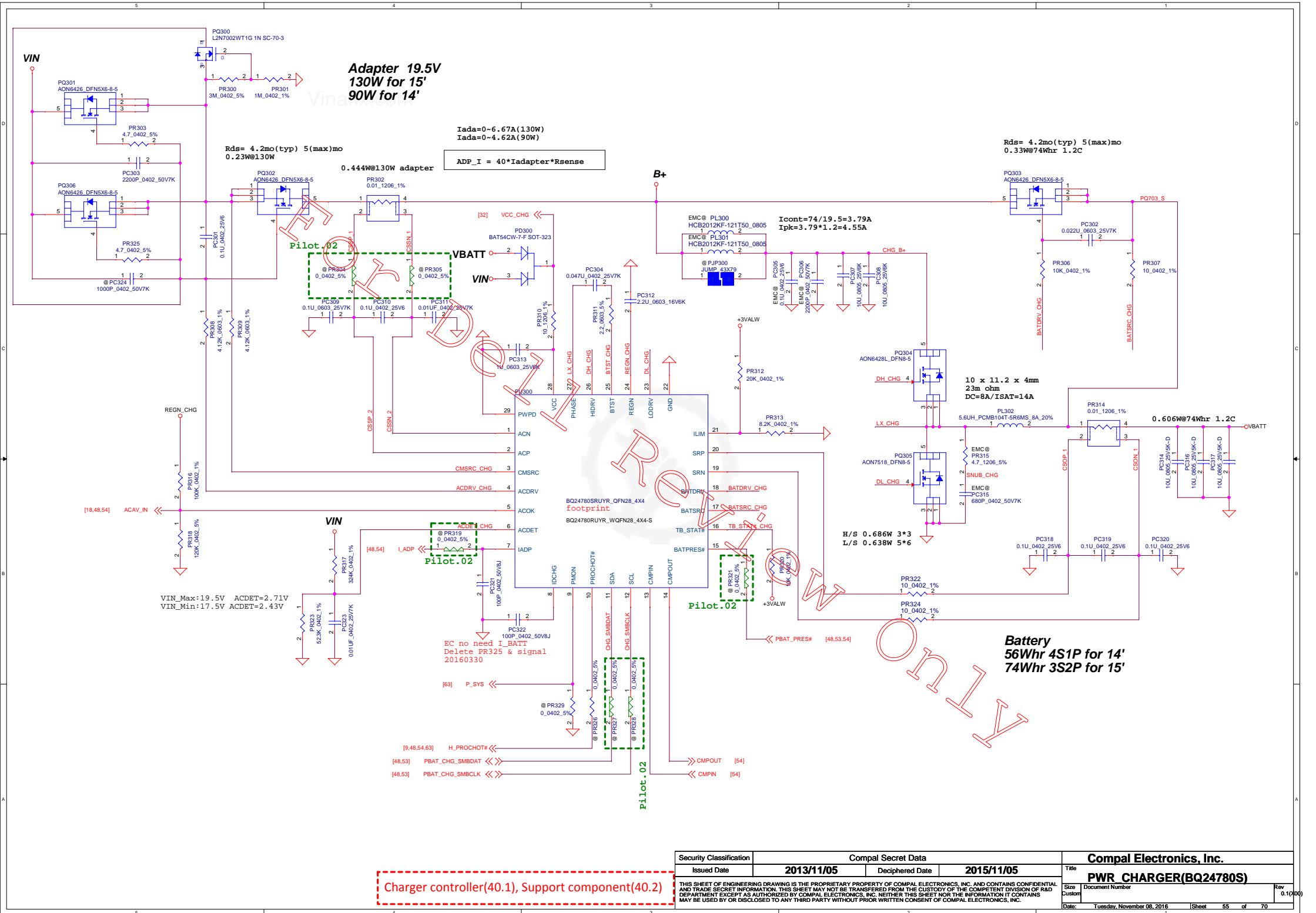


Erp lot 6 circuit

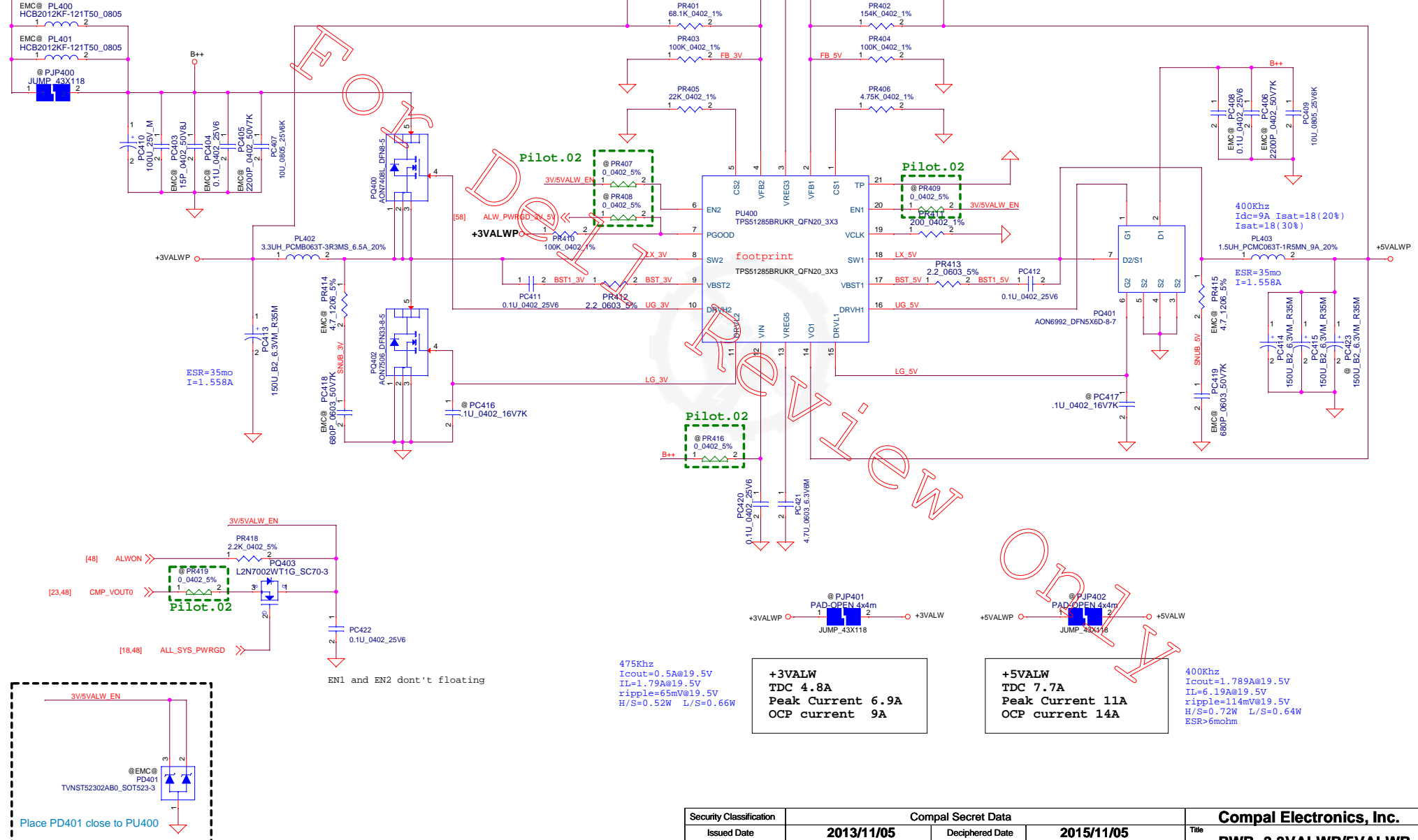


Ref ENG0012879 Circuit-4
HW Asserts H_PROCHOT# when battery
is being unplugged and keep low for 10ms
until SW prochot# is issued by EC

Rest of support elements (37.1)



$$(3.3 \times 8.1 + 10.5 \times 5) / 9 = 8.8$$



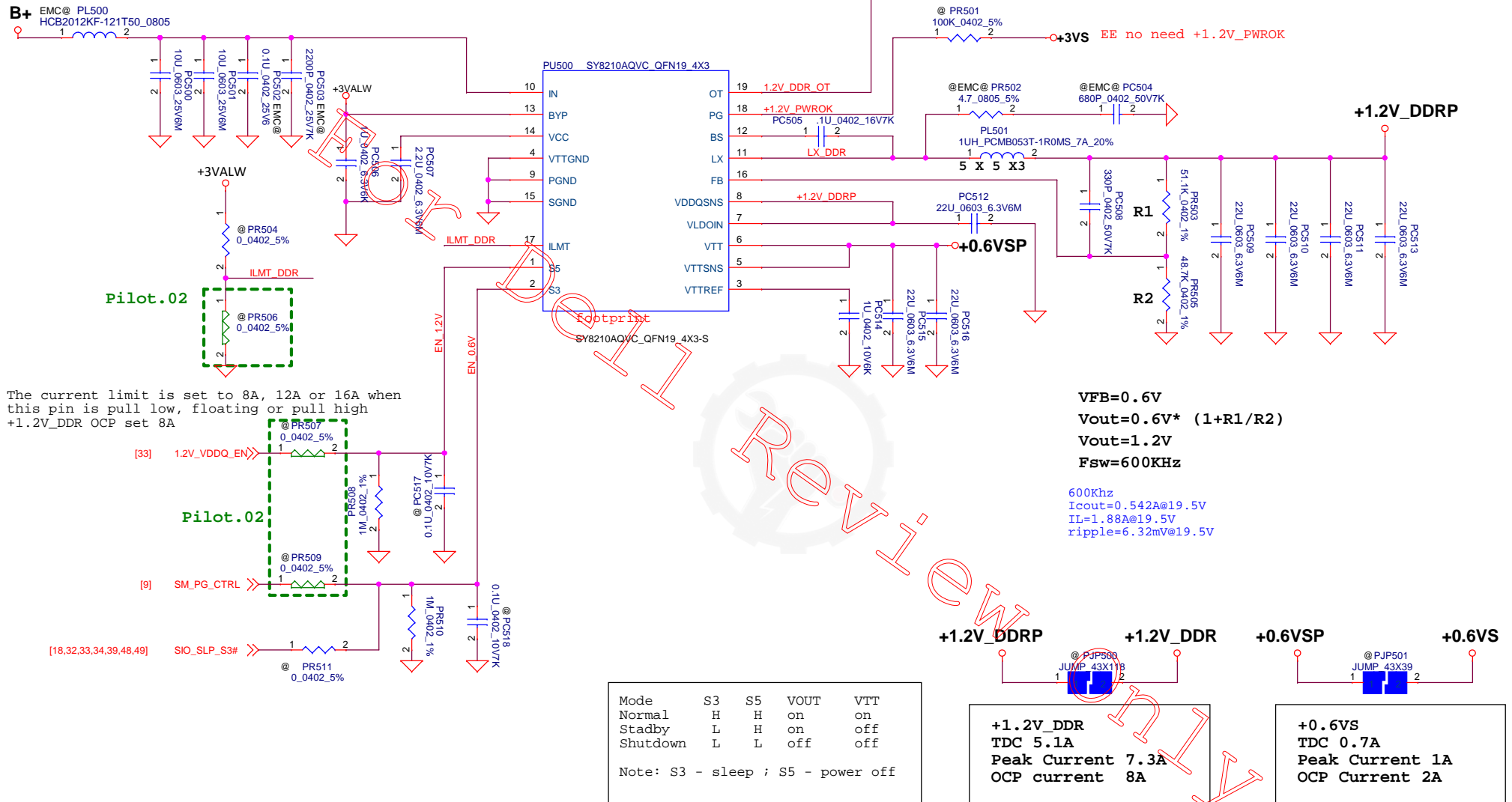
475Khz
I_{out}=0.5A@19.5V
I_L=1.79A@19.5V
ripple=65mV@19.5V
H/S=0.52W L/S=0.66W

+3VALW
TDC 4.8A
Peak Current 6.9A
OCP current 9A

+5VALW
TDC 7.7A
Peak Current 11A
OCP current 14A

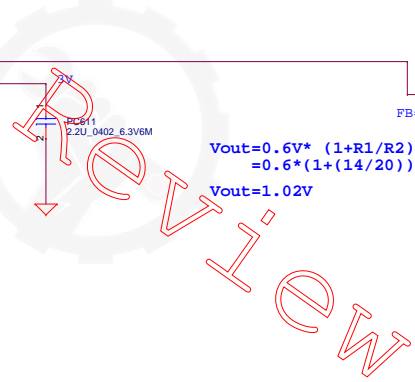
400Khz
I_{out}=1.789A@19.5V
I_L=6.19A@19.5V
ripple=114mV@19.5V
H/S=0.72W L/S=0.64W
ESR>6mohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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DDR controller(35.3), Support component(35.4)

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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	PWR +1.2V_DDR/0.6VS(SY8210)
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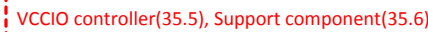
500Khz
IL=1.9A@19.5V
ripple=7.3mV@19.5V

$$V_{out} = 0.6V * (1 + R_1/R_2)$$
$$= 0.6 * (1 + (14/20))$$
$$V_{out} = 1.02V$$

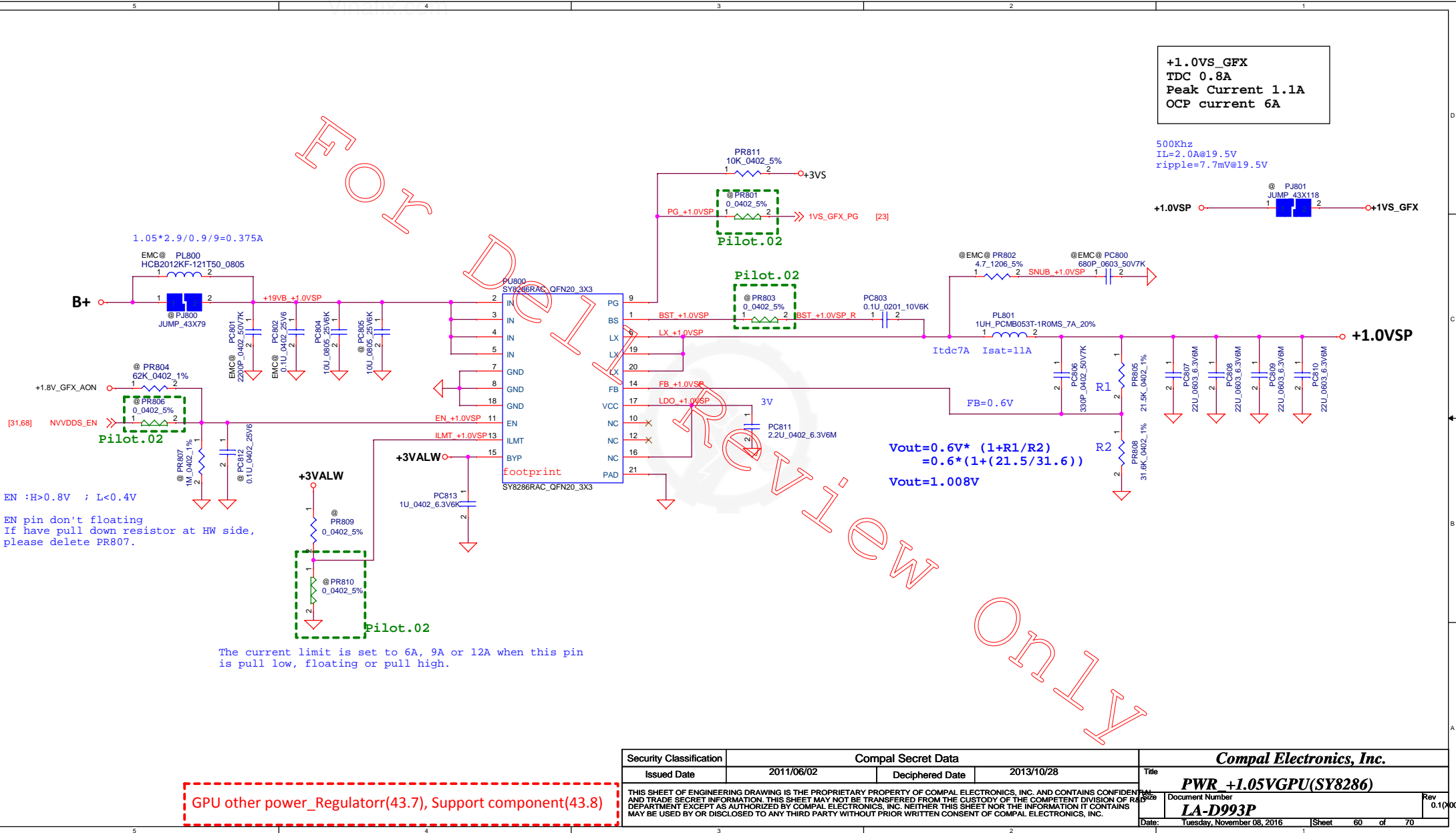
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Top Secret Data	
Deciphered Date	2013/1

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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+1.0VS_GFX
TDC 0.8A
Peak Current 1.1A
OCP current 6A

500Khz
IL=2.0A@19.5V
ripple=7.7mV@19.5V

+1.0VSP → [P801 JUMP 43X118] → +1VS_GFX

1.05*2.9/0.9/9=0.375A

+1.8V_GFX_AON

[31,68] NVVDDS_EN

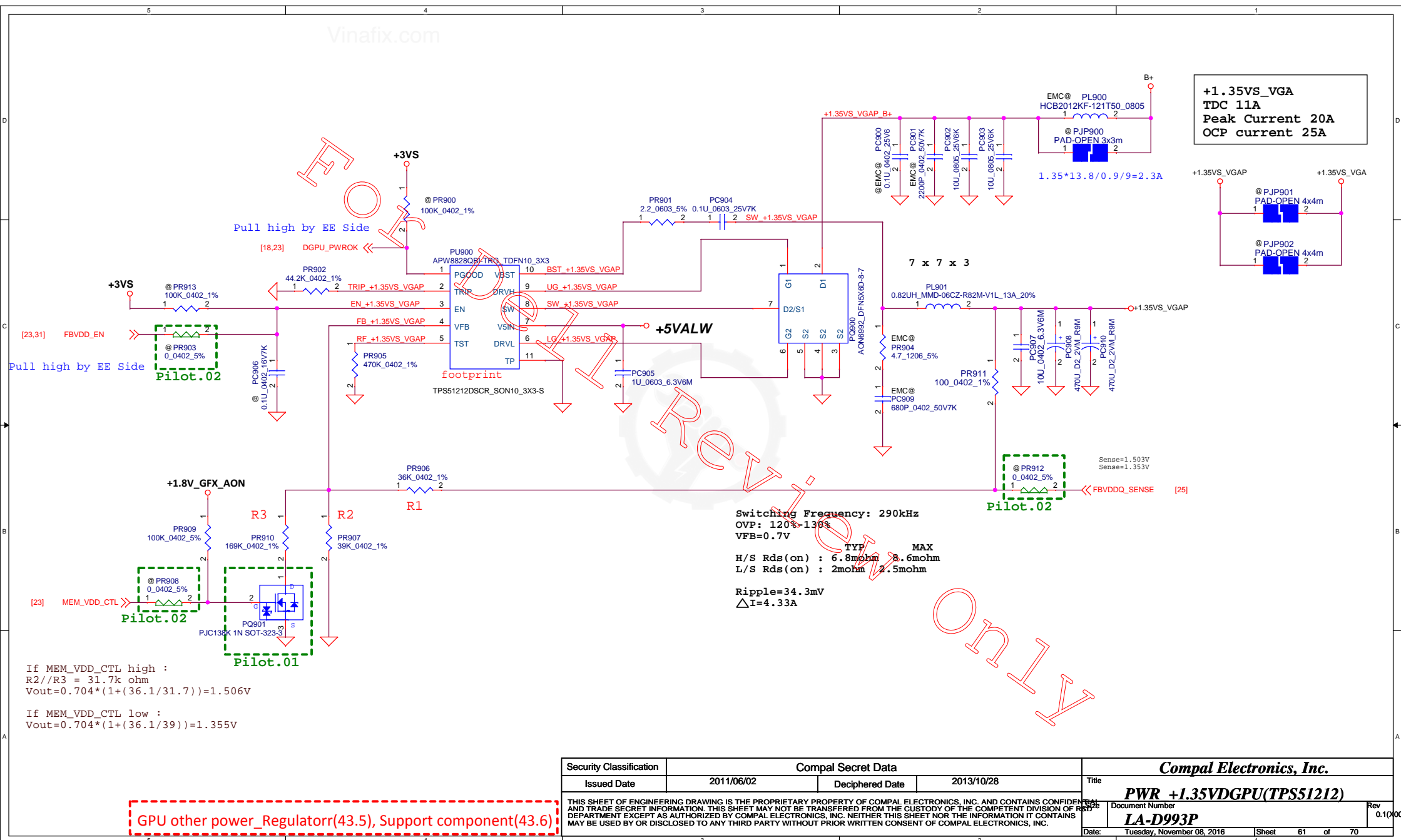
EN :H>0.8V ; L<0.4V
EN pin don't floating
If have pull down resistor at HW side,
please delete PR807.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

$$V_{out} = 0.6V * (1 + R1/R2)$$
$$= 0.6 * (1 + (21.5/31.6))$$
$$V_{out} = 1.008V$$

GPU other power_Regulatorr(43.7), Support component(43.8)

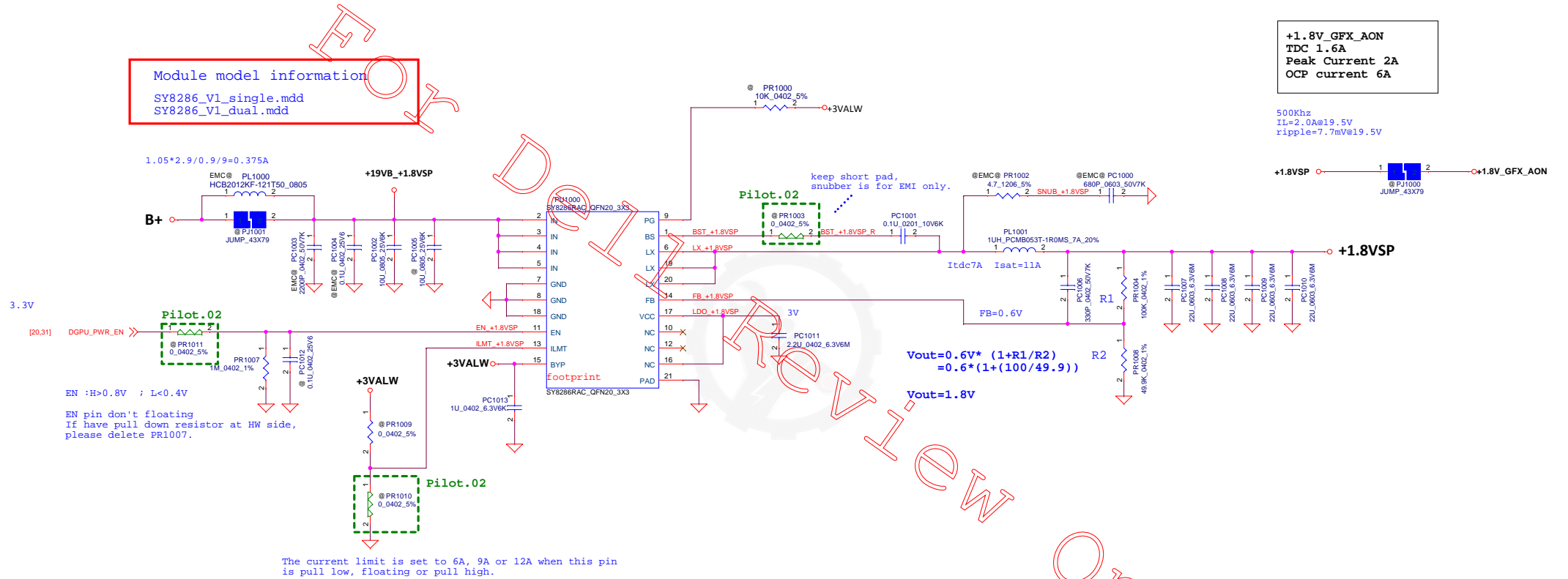
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	PWR +1.05VGPU(SY8286)
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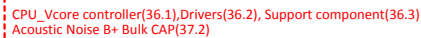


Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd

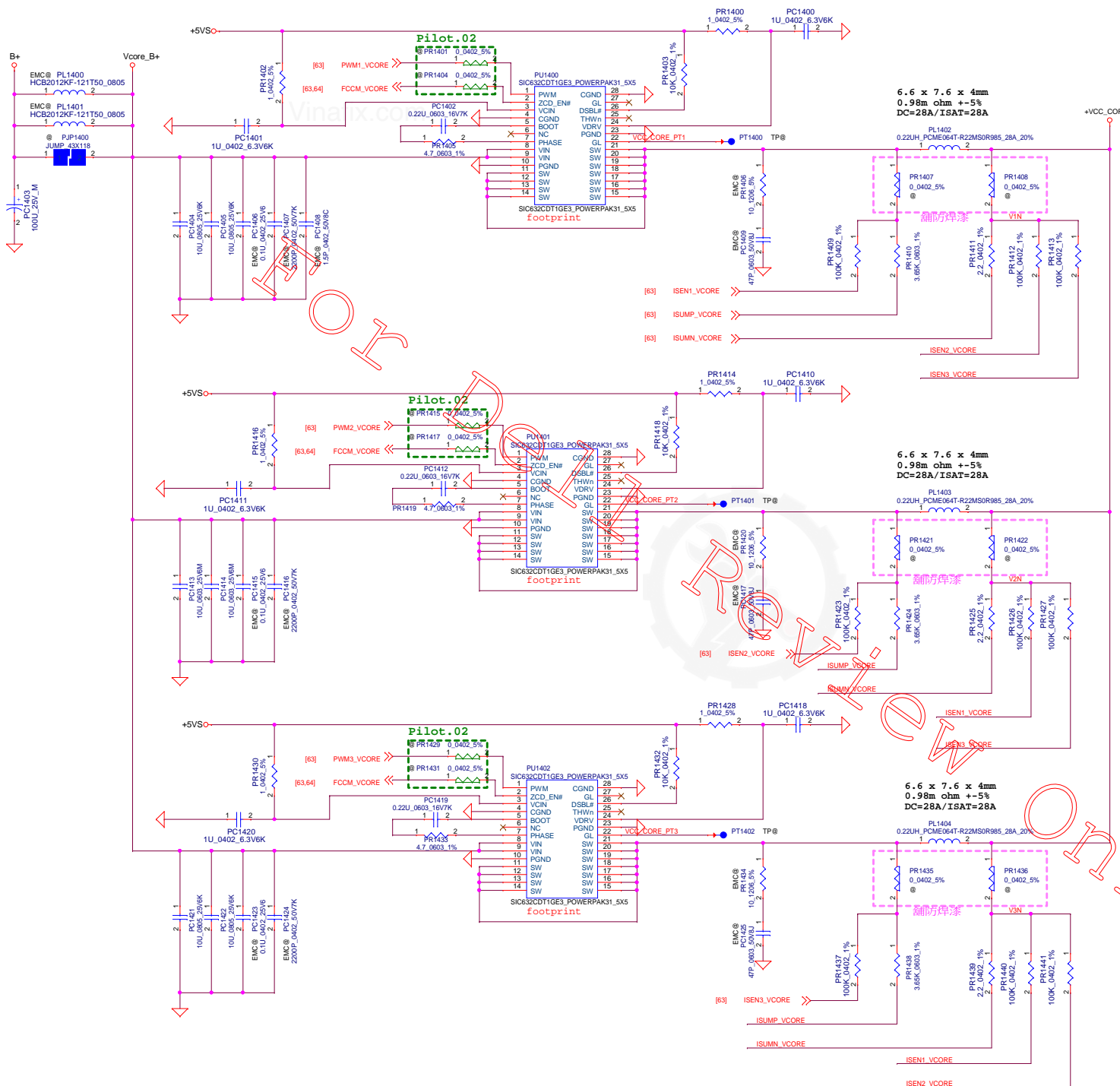
$$1.05 \times 2.9 / 0.9 / 9 = 0.375A$$





CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

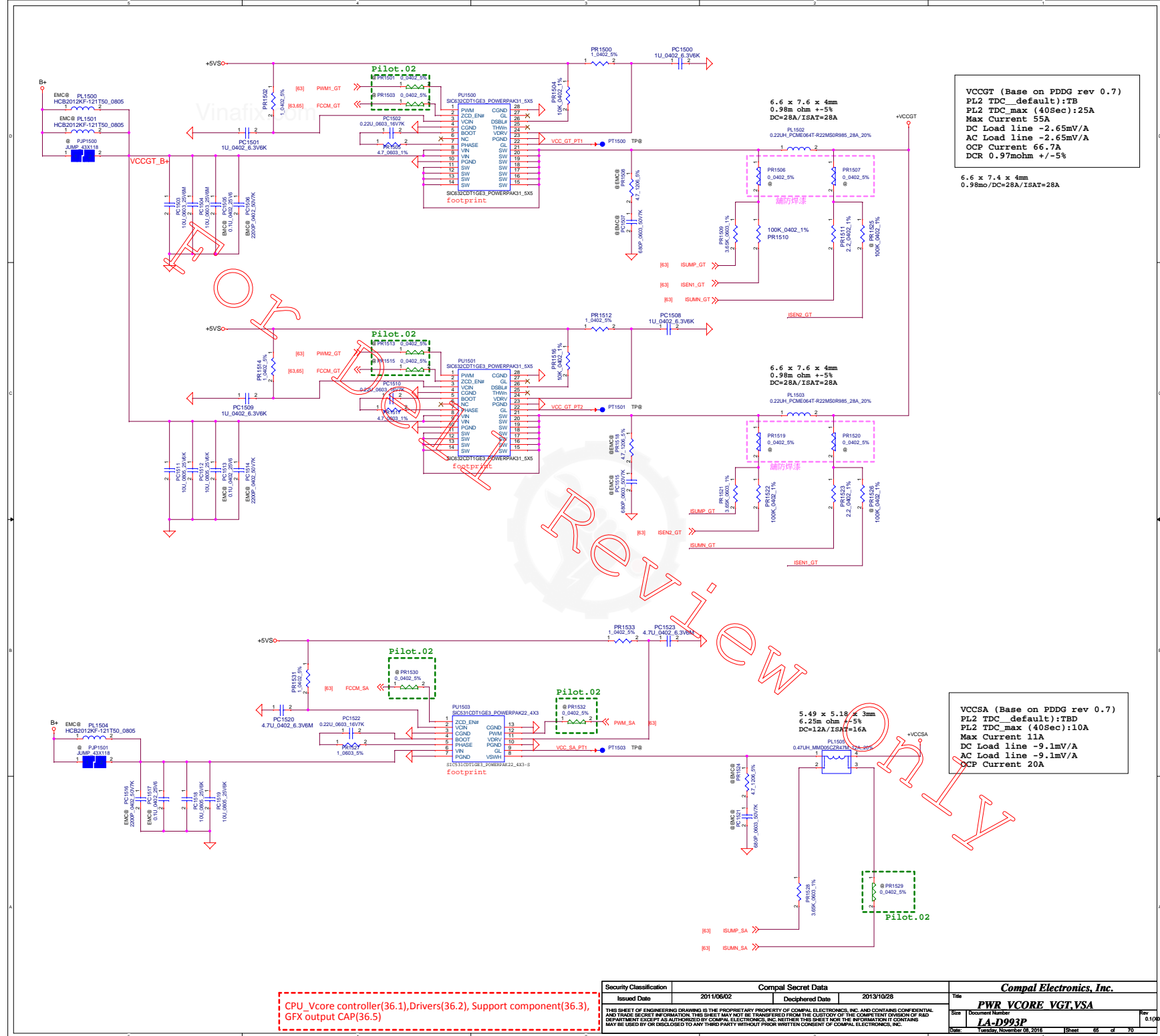
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<p>DATE: 10/29/2013 10:26 AM</p>			Size	Sheet 63 of 70
<p>DATE: 10/29/2013 10:26 AM</p>			Size	Sheet 63 of 70

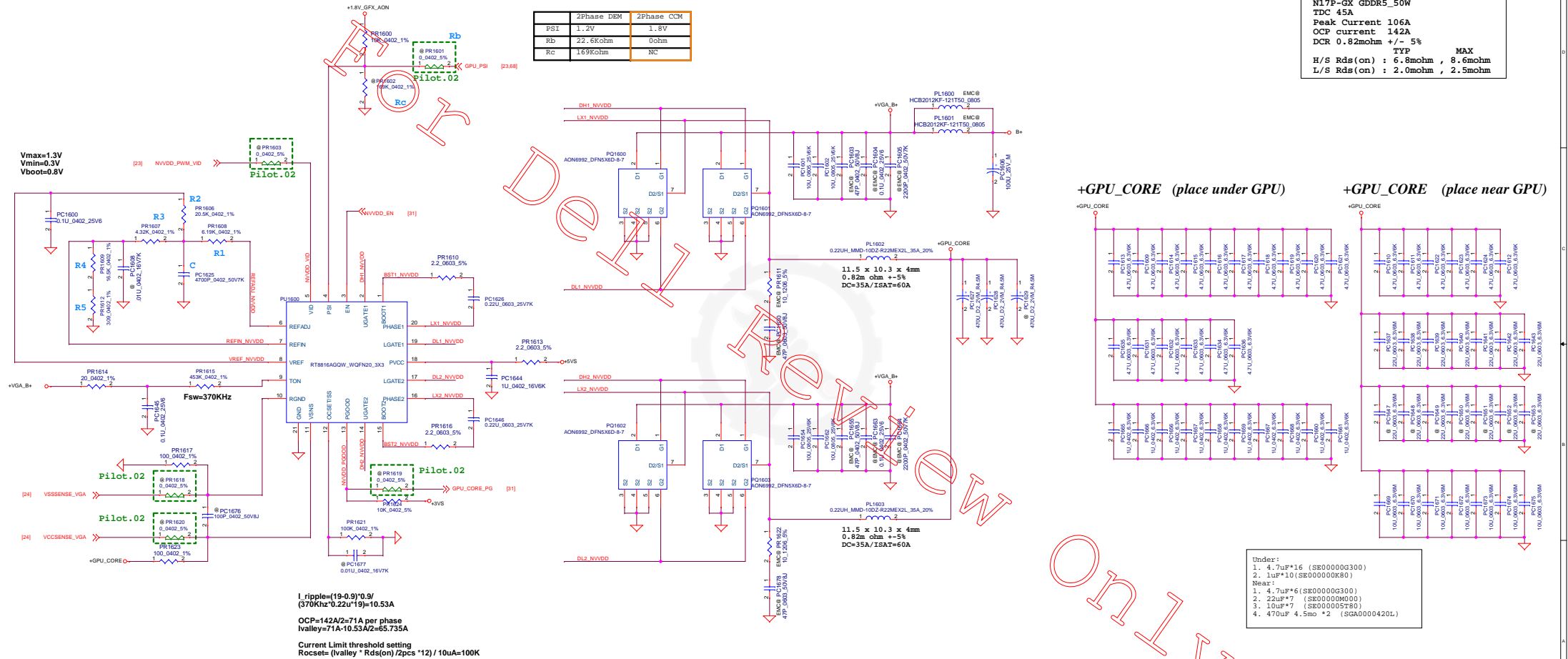


VCC_core (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):50A
 Peak Current 68A
 DC Load line -1.8mV/A
 AC Load line -1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

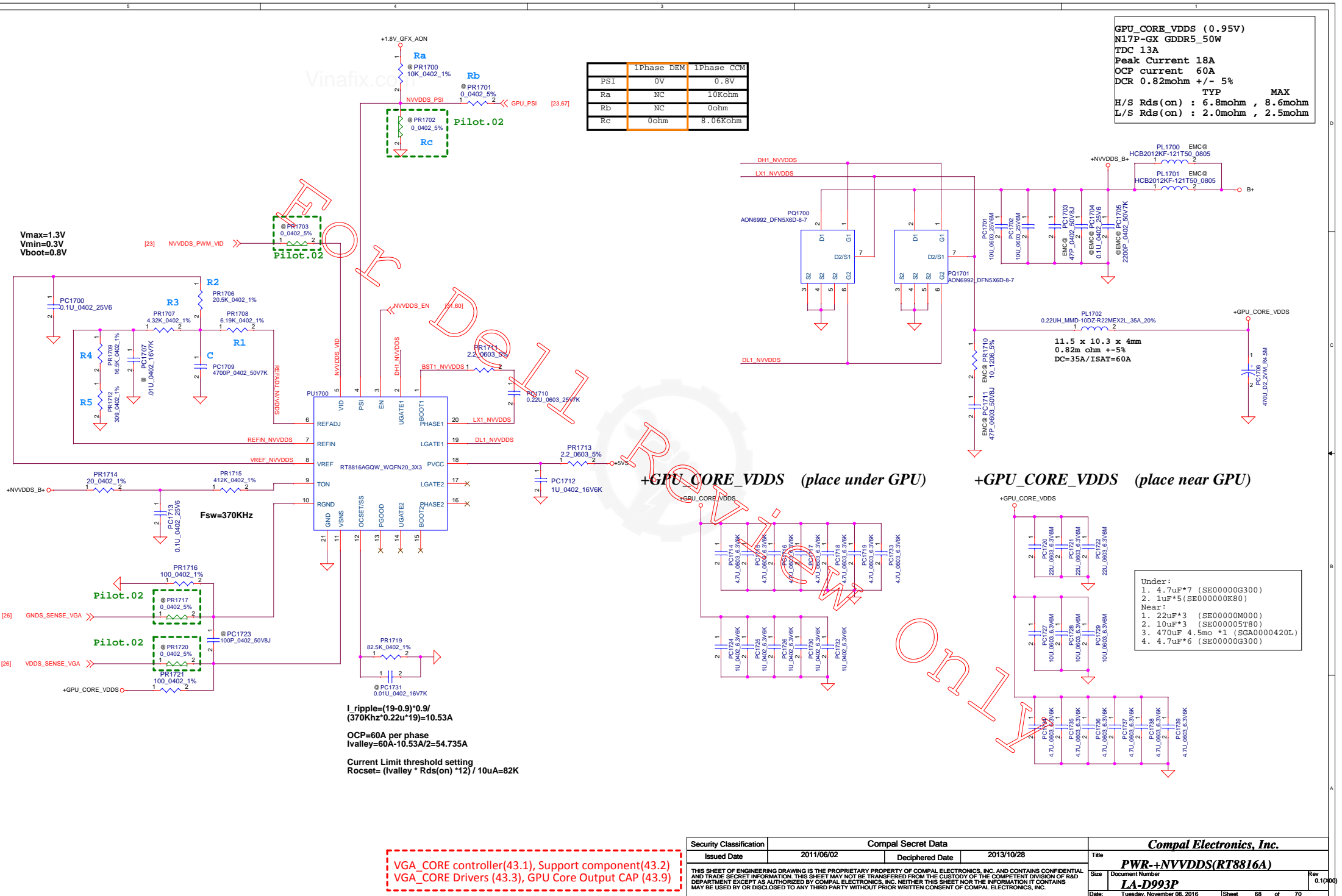
CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 CPU_Core output CAP(36.4), Acoustic Noise B+ Bulk CAP(37.2)

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				Version	01/00
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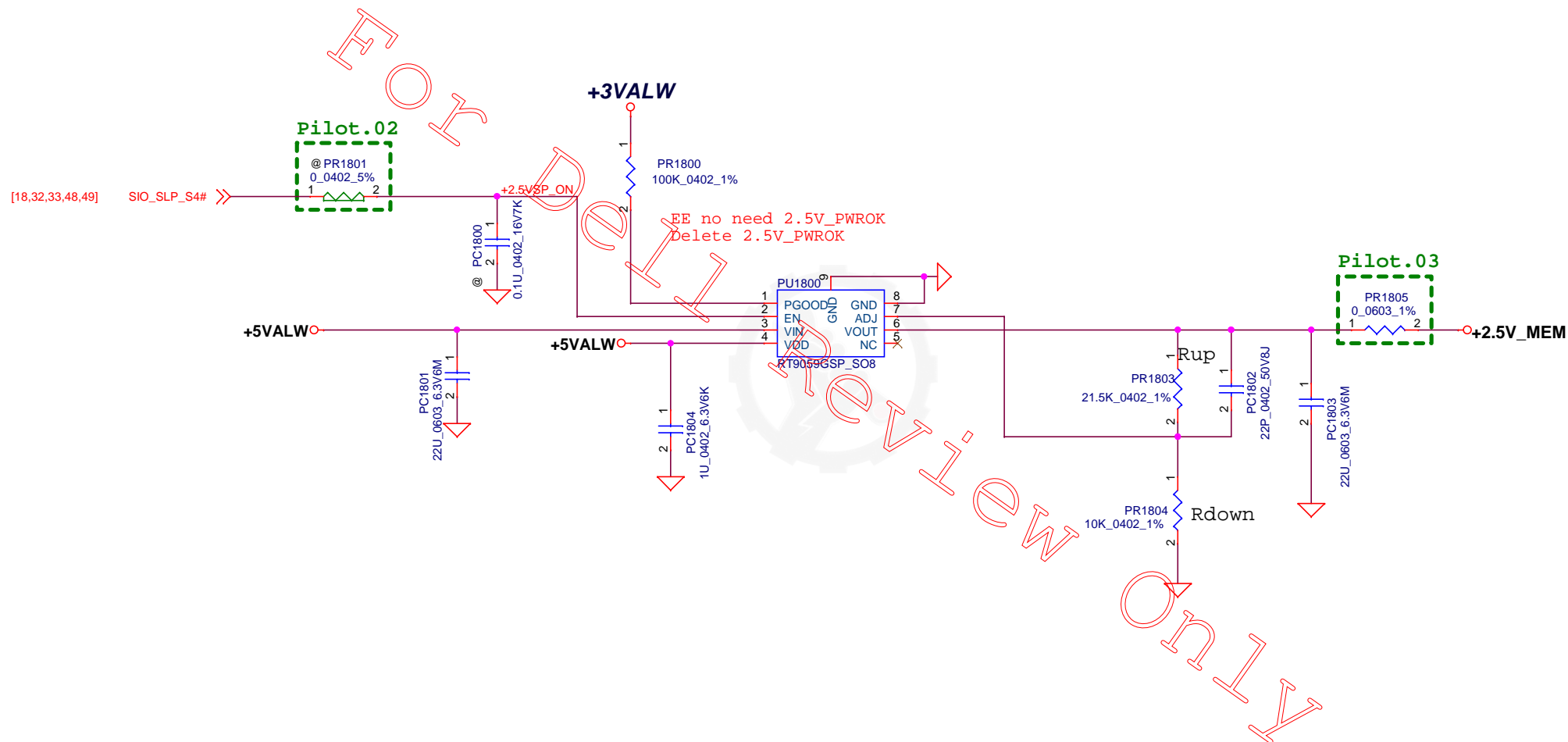
	1Phase DEM	1Phase CCM
PSI	0V	0.8V
Ra	NC	10Kohm
Rb	NC	0ohm
Rc	0ohm	8.06Kohm

GPU_CORE_VDDSS (0.95V)
N17P-GX GDDR5_50W
TDC 13A
Peak Current 18A
OCP current 60A
DCR 0.82mohm +/- 5%
H/S Rds(on) : 6.8mohm , 8.6mohm
L/S Rds(on) : 2.0mohm , 2.5mohm

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A



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